# BOLO8BLF
# Advance Product Specification


*High Performance Simultaneous Data Acquisition*

# Table of Contents

# 1 Product Description

1. ***BOLO8BLF*** is an 8 channel simultaneous analog I/O module for controlling and measuring Bolometers with typical resistance of 1.2kΩ.
2. Analog Inputs: 8 channels, 16 bit resolution, 1000kSPS/channel.
3. Differential bridge excitation common to all channels: 1000kSPS, 16 bit DAC. Typical output is ±10V @ 20kHz.
4. Calibration: 8 channel single-ended DAC, 16 bit resolution, 2kSPS typical use case. Current measurement at 16 bit resolution, 1kSPS typical use case.
5. Extended module with *FMC* connector. 4x RJ45 connectors for ease of connection; 2 Bolometers per connector.
6. Differential inputs, high quality differential amplifier front end with switched input voltage ranges.

## *1.1 Overview*

The *BLF* module standard adds user IO to carrier modules fitted with *FPGA* resource. D-TACQ recommends modules based on the *Xilinx ZYNQ* system on chip, combining *FPGA* resource with a dual-core ARM Cortex A9 and gigabit Ethernet. Compatible modules include

- D-TACQ ***ACQ1001*** : D-TACQ single slot *FMC* carrier, Z7020
- D-TACQ ***ACQ1002*** : D-TACQ dual slot *FMC* carrier, Z7020
- D-TACQ ***ACQ2006*** : D-TACQ 6 slot *FMC* carrier, Z7020
- D-TACQ ***ACQ2106*** : D-TACQ 6 slot *FMC* carrier, Z7030

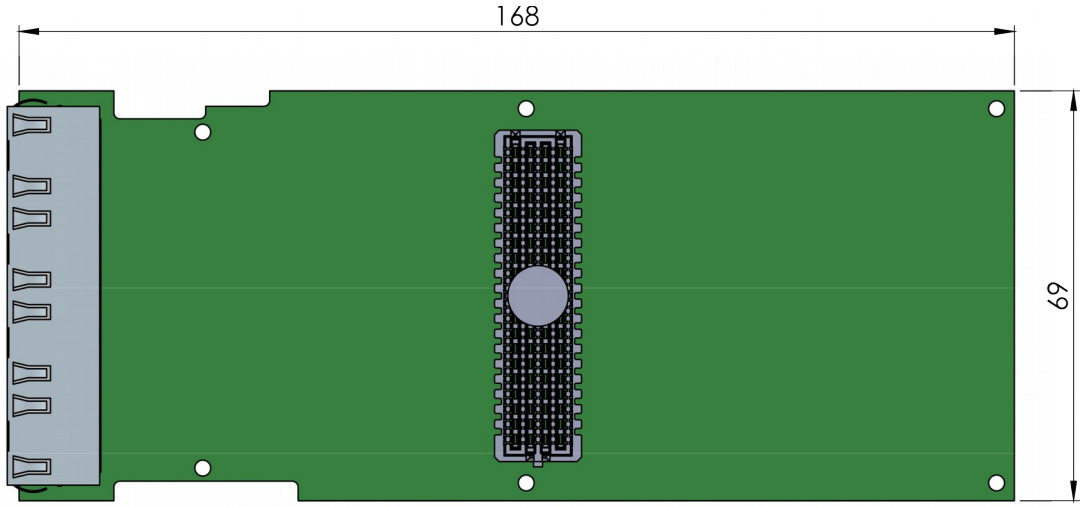
D-TACQ supplies a complete working Intelligent Digitizer appliance including programmable logic and microprocessor system running Linux.

## *1.2 Glossary*

- *FMC*: VITA57 FPGA Mezzanine Card.
- Xilinx ZYNQ System-on-chip.
- *LPC* : *FMC* Low pin count wiring standard.
- *ULPC*: *FMC* Ultra low pin count (D-TACQ).
- ELF: D-TACQ extension to FMC, elongated card to the rear with provision for dedicated analog power supply rails.
- BLF: D-TACQ extension to FMC, elongated card to front and rear with provision for dedicated analog power supply rails.

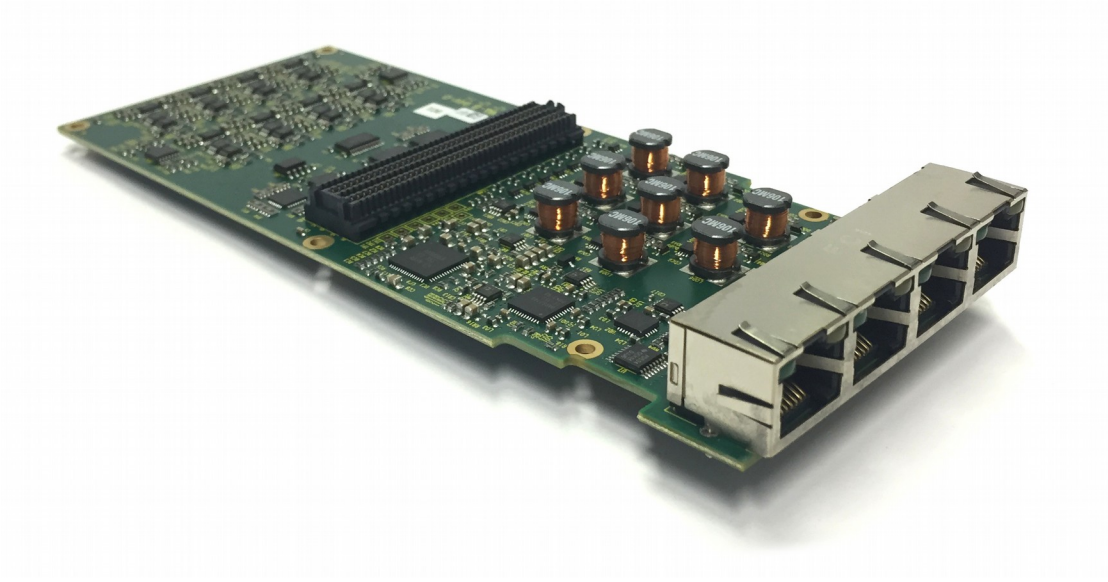
# 2 Physical

## 2.1 BLF Extended FMC Module

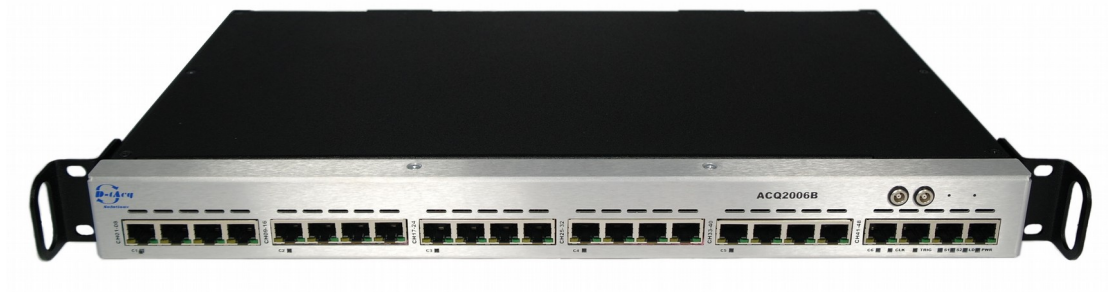



*Drawing 1: BOLO8BLF Dimensions*

## 2.2 Appearance



*Drawing 2: BOLO8BLF*



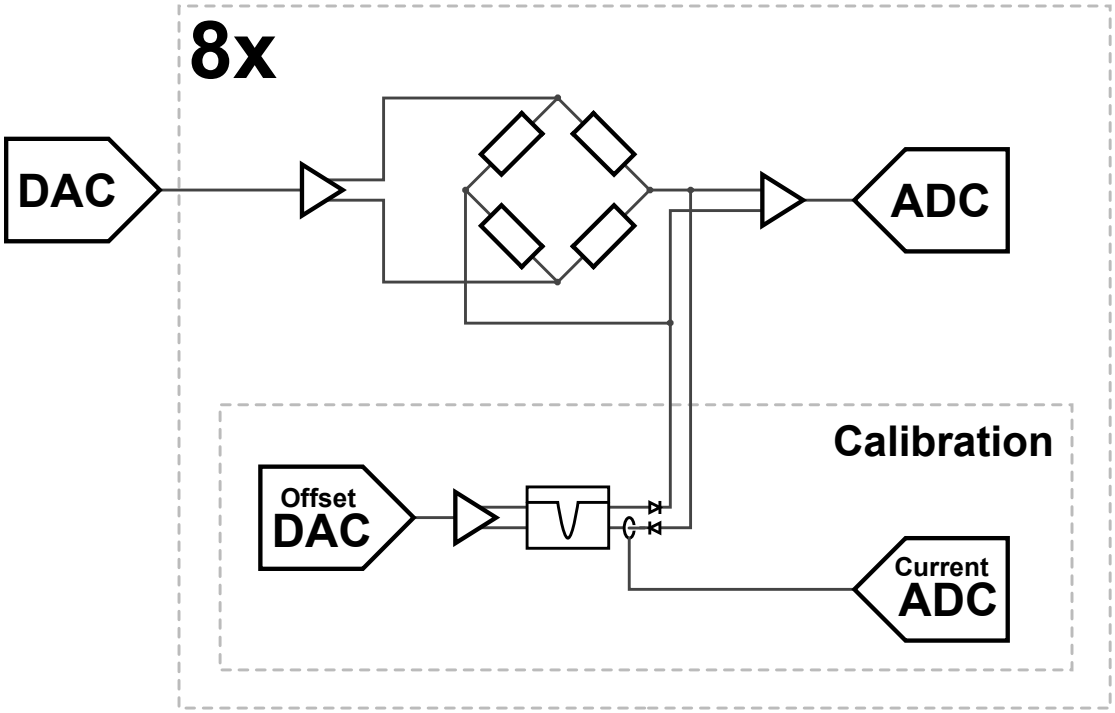

*Drawing 3: 6x BOLO8BLF in ACQ2006 - 48 Channel System*

# 3 Theory of Operation

The main DAC excites all eight Bolometer bridges. Each Bolometer has an individual ADC to digitise the incoming data.

Calibration is performed by forward-biasing the Offset DACs and measuring the resulting current. A 20kHz Bandstop filter separates the offset DAC from the excitation.

A comprehensive FPGA control personality is under development at CCFE.




*Drawing 4: BOLO8BLF Block Diagram – Bridge is shown for reference.*

# 4 BOLO8BLF Interface Specification

## *4.1 Front Panel Connector*

- 4x RJ45 connectors. Input/Output pairing is configured to use standard ethernet cable differential pairing for ease of wiring.

### 4.1.1 Pinout

Each RJ45 connector is identical in pinout.

| **Pin** | **Function** |
|---|---|
| 1 | +Channel A In (+Offset DAC Out) |
| 2 | -Channel A In (-Offset DAC Out) |
| 3 | +Channel A Excitation Out |
| 4 | -Channel B Excitation Out |
| 5 | +Channel B Excitation Out |
| 6 | -Channel A Excitation Out |
| 7 | +Channel B In (+Offset DAC Out) |
| 8 | -Channel B In (-Offset DAC Out) |

# 5 BOLO8BLF Electrical Specification

## *5.1 Main ADCs*

| # | Parameter | Value |
|---|---|---|
| 1 | Number of Channels | 8 |
| 2 | Sample Rate | 1MHz<br>per channel simultaneous |
| 3 | Resolution | 16 bits |
| 4 | Coupling | DC, Differential Input |
| 5 | Input Impedance | 1M |
| 6 | Input Voltage Range | ±10, ±5, ±2.5, ±1.25 V<br>software selectable ranges |
| 7 | Input Voltage Withstand | ±30V |
| 8 | Offset Error | 0.01% FS with numerical calibration |
| 9 | Gain Error | 0.01% FS with numerical calibration |
| 10 | INL | 16 bit ±0.5 LSB |
| 11 | DNL | 16 bit ±0.1 LSB |
| 12 | CMRR | >80dB FS @ 1 kHz |
| 13 | THD (Gain x1) | -98 dB* |
| 14 | SINAD (Gain x1) | -93 dB* |
| 15 | SFDR | 100 dBc* |
| 16 | SNR<br>Gain x1<br>Gain x2<br>Gain x4<br>Gain x8 | <br>94.46 dB*<br>94.12 dB*<br>92.36 dB*<br>89.61 dB* |
| 17 | Full Power BW (Gain x1) | 100kHz |
| 18 | Small Signal BW (Gain x1) | 1MHz |
| | Crosstalk (Gain x1) | <90 dB @ 1 kHz FS Input |
| | Temperature Stability | <25 ppm/C |

Typical values

* Typical values measured at full scale with a 9.76kHz input

## *5.2 Main DAC*

| # | **Parameter** | **Value** |
|---|---|---|
| 1 | Number of Channels | 1 (split into 8 channels) |
| 2 | Sample Rate | Up to 1000 kHz,<br>per channel simultaneous |
| 3 | Resolution | 16 bits |
| 4 | Coupling | DC, Differential Output |
| 5 | Maximum output current | 20mA per channel |
| 6 | Output Voltage Range | ±10 V |
| 7 | Output Impedance | 33Ω |
| 8 | Offset Error | 0.01% FS with numerical calibration |
| 9 | Gain Error | 0.01% FS with numerical calibration |
| 10 | INL | ±2 LSB |
| 11 | DNL | ±1 LSB |
| 12 | THD | 92 dB |
| 13 | SINAD | 89 dBc |
| 14 | SFDR | 95 dBc |
| 15 | SNR | 90 dB |
| 16 | Full Power BW | 200kHz Standard |
| | Crosstalk | <95 dB @ 1 kHz FS |
| | Temperature Stability | <25 ppm/C |
| | | |

Typical values

## *5.3 Offset DAC*

| # | **Parameter** | **Value** |
|---|---|---|
| 1 | Number of Channels | 8 |
| 2 | Sample Rate | 2kHz,<br>per channel simultaneous |
| 3 | Resolution | 16 bits |
| 4 | Coupling | DC, Differential Output |
| 5 | Maximum output current | 20mA per channel |
| 6 | Output Voltage Range | ±7.5 V |
| 7 | Output Impedance | 33Ω |
| 8 | Offset Error | 0.03% FS with numerical calibration |
| 9 | Gain Error | 0.03% FS with numerical calibration |
| 10 | INL | ±4 LSB |
| 11 | DNL | ±1 LSB |
| 12 | Full Power BW | 1kHz Standard |
| 13 | Crosstalk | <85 dB @ 1 kHz 4Vpp (TBD) |
| | Temperature Stability | <25 ppm/C |
| | | |

Typical values

## *5.4 Current ADC*

| # | **Parameter** | **Value** |
|---|---|---|
| 1 | Number of Channels | 8 |
| 2 | Sample Rate | 1kHz<br>per channel simultaneous |
| 3 | Resolution | 16 bits |
| 4 | Coupling | DC, Single-ended Input |
| 5 | Input Impedance | 1M |
| 6 | Input Current Range | ±10mA |
| 7 | Input Voltage Withstand | ±30V |
| 8 | Offset Error | 0.03% FS with numerical calibration |
| 9 | Gain Error | 0.25% FS with numerical calibration |
| 10 | INL | 16 bit ±0.2 LSB typ. |
| 11 | DNL | 16 bit ±0.2 LSB typ. |
| 12 | THD | -80dB (TBD) |
| 13 | SINAD | 70dB (TBD) |
| 14 | SFDR | 80dB (TBD) |
| 15 | SNR | 70dB (TBD) |
| 16 | Full Power BW | 1kHz |
| 17 | Crosstalk | <90 dB @ 1 kHz FS Input |
| | Temperature Stability | <25 ppm/C |

Typical values

# 6 BOLO8BLF Specification

| # | Parameter | Value |
|---|---|---|
| 1 | Form Factor | D-TACQ Standard BLF |
| 2 | Power source | D-TACQ ELF/BLF Module – Please contact us if details are required. |
| 3 | Environmental | 0°C-50°C Operational<br>-10°C-85°C Non-Operational |
| 4 | ELF Socket | Standard ELF D-TACQ Ultra Low Pin Count ULPC |