

ACQ400 FIR Filters Guide

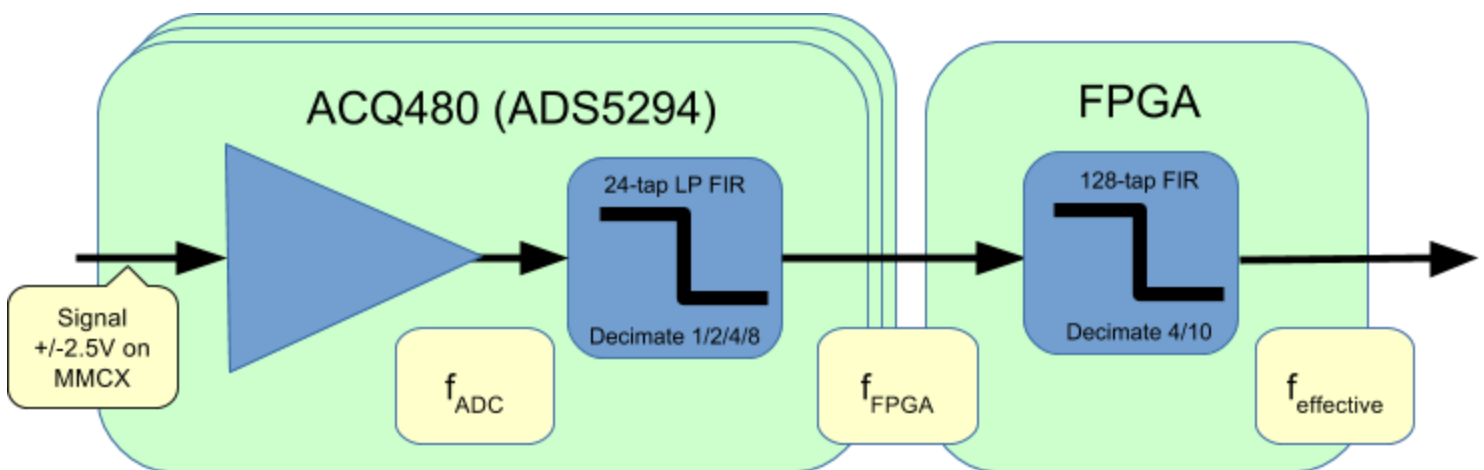
This document describes the FPGA FIR Filter implementation on D-TACQ ACQ400 Series products. An overview of the filters and the steps required for end users to control them is given.

D-TACQ Filter Architecture Block Diagram

The ACQ480 filtering is split into two stages. There is a small programmable FIR filter on the ADC device itself, and a larger, more capable FIR filter implemented in the FPGA fabric.

This provides two stages for potential decimation and data reduction, whilst the ADCs are still sampling at full rate.

The various sampling rates throughout the decimation change are named as indicated below. These names are useful when providing worked examples; included later in this document.



ACQ480 ADS5294 FIR Filters

The ADS5294 ADC has some DSP features on board. These include built in FIR decimating filters.

Filter Characteristics

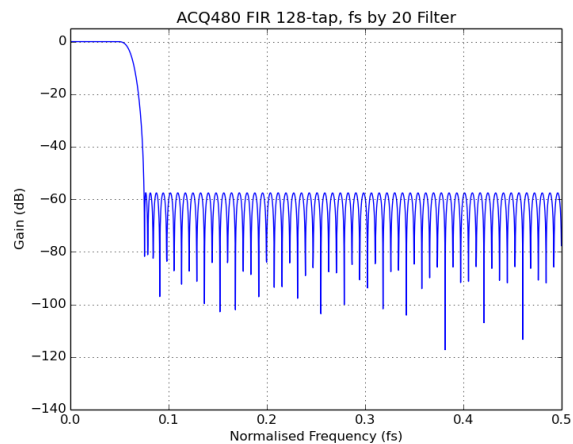
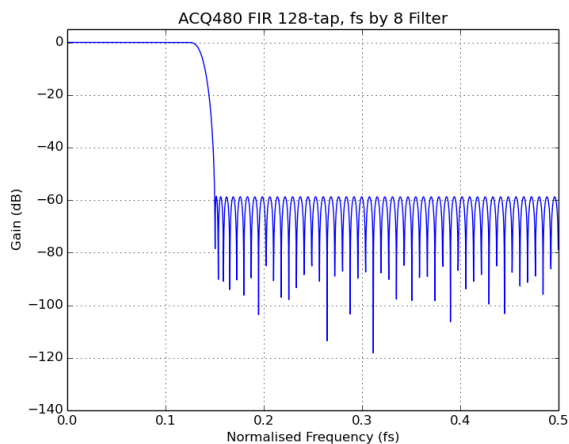
- 24 taps
- Symmetric
- 12-bit Signed coefficients
- Decimation?
 - Decimate by 1, 2, 4 & 8

ACQ480 FPGA FIR Filters

The ACQ480 product utilises hardware FIR filters in the FPGA logic as a means to reduce the data rate, through oversampling, or to make SNR improvements through narrowing the signal bandwidth.

Filter Characteristics

- 25 MHz Maximum Sample Rate
- 128 taps
- Symmetric
- 20-bit Signed coefficients
- Decimation?
 - 2 FPGA personalities. Decimate by 4 or 10. This is a boot time switch



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Setup Filter Coefficients

In order to begin using the filtering options presented above a support package must first be installed. A user can access the D-TACQ command line over ssh or through a serial comms connection.

Install Package

Move the new package to the /mnt/packages directory and reboot the D-TACQ box.

```
mv /mnt/packages.opt/90-custom_acq480fir* /mnt/packages
```

A new directory is created at /usr/local called **coeff_sets**.

This contains a set of useful coefficients for each FIR.

ADS5294:

total 192

-rwxr-xr-x	1	root	root	75	Aug	5	14:22	by16
-rwxr-xr-x	1	root	root	76	Aug	5	14:22	by32
-rwxr-xr-x	1	root	root	75	Aug	5	14:22	by4
-rwxr-xr-x	1	root	root	75	Aug	5	14:22	by8
-rwxr-xr-x	1	root	root	58	Aug	5	14:22	half_amp
-rwxr-xr-x	1	root	root	59	Aug	5	14:22	unity_gain

DEC10:

total 128

-rwxr-xr-x	1	root	root	387	Aug	5	14:22	default
-rwxr-xr-x	1	root	root	165	Aug	5	14:22	
half_amplitude								
-rwxr-xr-x	1	root	root	377	Aug	5	14:22	half_nyq
-rwxr-xr-x	1	root	root	165	Aug	5	14:22	unity_gain

DEC4:

total 96

-rwxr-xr-x	1	root	root	353	Aug	5	14:22	default
-rwxr-xr-x	1	root	root	350	Aug	5	14:22	half_nyq
-rwxr-xr-x	1	root	root	133	Aug	5	14:22	unity_gain

Select Custom ADS5294 Filter

From Control System Studio (CSS) open the ACQ480 opi for the relevant site.

ACQ480FMC acq2106_007:1

CH	INVERT	GAIN	HP FILTER	LFNS	50R	FIR
ALL					<input type="checkbox"/>	DISABLE
01	OFF <input type="checkbox"/>	0 dB	OFF	OFF <input type="checkbox"/>	<input type="checkbox"/>	
02	OFF <input type="checkbox"/>	0 dB	OFF	OFF <input type="checkbox"/>	<input type="checkbox"/>	
03	OFF <input type="checkbox"/>	0 dB	OFF	OFF <input type="checkbox"/>	<input type="checkbox"/>	
04	OFF <input type="checkbox"/>	0 dB	OFF	OFF <input type="checkbox"/>	<input type="checkbox"/>	
05	OFF <input type="checkbox"/>	0 dB	OFF	OFF <input type="checkbox"/>	<input type="checkbox"/>	
06	OFF <input type="checkbox"/>	0 dB	OFF	OFF <input type="checkbox"/>	<input type="checkbox"/>	
07	OFF <input type="checkbox"/>	0 dB	OFF	OFF <input type="checkbox"/>	<input type="checkbox"/>	
08	OFF <input type="checkbox"/>	0 dB	OFF	OFF <input type="checkbox"/>	<input type="checkbox"/>	

Link Status
ACQ480_ACTIVATE

FFIR Decim 4

Output Sample Rate
2.5004E6 Hz

Output Sample Count
2.6776E9

DISABLE
LP_ODD_D2
HP_ODD_D2
LP_EVEN_D4
BP1_EVEN_D4
BP2_EVEN_D4
HP_ODD_D4
CUSTOM_D2
CUSTOM_D4
CUSTOM_D8
CUSTOM_D1

The bottom 4 options in the dropdown menu, with prefix CUSTOM, allow the user to select a decimation factor (1,2,4,8) and apply the custom filter coefficients which will be loaded in the next step.

Note the "FFIR (FPGA FIR) Decim" field reports the internal decimation within the FPGA.

Or set programmatically

```
set.site 1 ACQ480:FIR:01 FILTYPE
```

Where FILTYPE : one of {

DISABLE,

LP_ODD_D2, HP_ODD_D2,

LP_EVEN_D4, BP1_EVEN_D4, BP2_EVEN_D4, HP_ODD_D4,

CUSTOM_D2, CUSTOM_D4, CUSTOM_D8, CUSTOM_D1 }

Loading Coefficients

FPGA Filter Load

To load a coefficient set into the FPGA FIR execute the following line :

```
acq2106_007> /usr/local/CARE/load.ffir /usr/local/coeff_sets/DECX/half_nyq
using file /usr/local/coeff_sets/DEC4/half_nyq
```

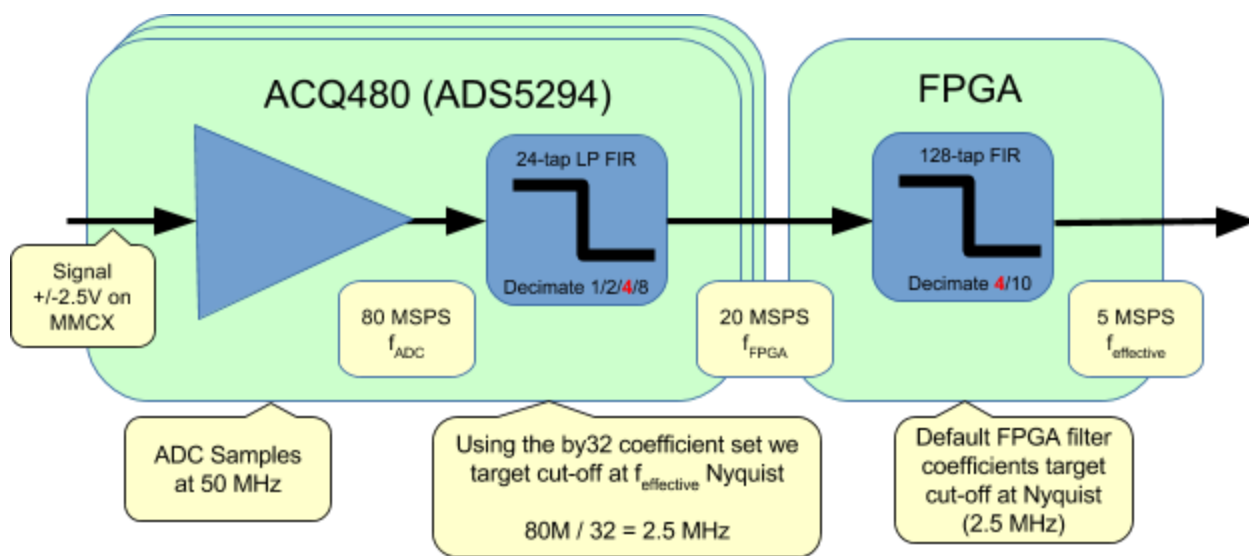
ADS5294 Filter Load

To load a coefficient set into the ADS5294 FIR, load any of the supplied coefficient sets from /usr/local/coeff_sets/ADS5294 by name (or specify another file name to load custom settings).

```
acq2106_007> /usr/local/CARE/load.acq480.fir by8
```

In the above example, the by8 coefficient set describes a filter whose cut-off begins at 1/8th of the normalised sampling frequency. These can be combined with the decimation rate to produce Nyquist or half Nyquist cutoff points.

- E.g.
 - Sampling Rate or f_s or f_{ADC} = 80 MHz
 - ADS5294 Decimation = 4
 - Effective ADS5294 Rate or f_{FPGA} = 20 MHz
 - FPGA Decimation = 4
 - Effective FPGA Rate or $f_{effective}$ = 5 MHz



by32 would produce a cutoff at Nyquist $80/32 = 2.5$ MHz
by64 would produce a cutoff at $\frac{1}{2}$ Nyquist $80/64 = 1.25$ MHz

Custom User Coefficients

It's possible for users to roll their own filter coefficients. Contact D-TACQ for details.