

# ACQ423ELF

32 Channel Simultaneous Analog Input Module



## Product Description

- 32 channel simultaneous inputs
- 16 bit resolution
- Programmable Input Voltage Range
- High SNR typical 90dB
- Software channel masking for higher sample rate, options:
  - 32 Channels Enabled, Fs = 200ksps
  - 16 Channels Enabled, Fs = 350ksps

## Digitiser Key Features

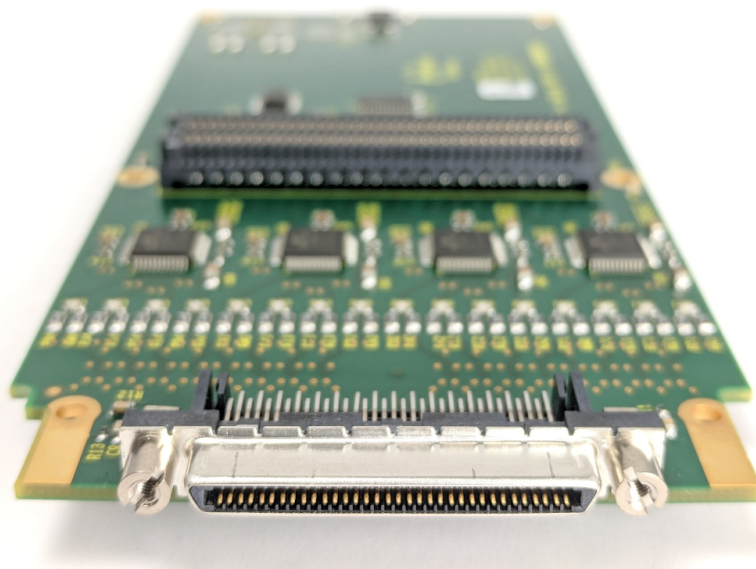
- Ideal for Instrumentation applications, control and monitoring
- Compatible with all D-TACQ Carriers offering up to 192 channels in a 1U 19" system
- Wide range of triggering and capture modes
- Compatible with a range of D-TACQ Breakout Panels and Termination Modules
- Internal FFC connectors for possible OEM Termination or Signal Conditioning

## Platform Key Features

D-TACQ supplies a complete working Intelligent Digitizer Appliance providing:

- FPGA based system with a range of flexible and customisable features
- Microprocessor system running open source Linux
- Comprehensive API provided in Python
- Onboard EPICS IOC for rapid integration

Please contact [info@d-tacq.com](mailto:info@d-tacq.com) for details on the above system integration options.



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## Glossary

- FMC : VITA57.1 FPGA Mezzanine Card
- ELF : Electrically Extended FMC, implies ULPC or DULPC (only compatible with D-TACQ carriers)
- LPC : FMC Low Pin Count standard as per VITA57.1
- ULPC : Subset by D-TACQ, Ultra Low Pin Count
- DULPC : Subset by D-TACQ, Differential Ultra Low Pin Count (ULPC with extra differential signalling)
- ZYNQ: Xilinx System on Chip (SoC) + FPGA logic
- FPGA : Field Programmable Gate Array

## 1 Product Description

1. ACQ423ELF is a minimum cost 32 channel simultaneous analog input module, intended to replace obsolete high channel count digitizers operating in the range 10..200kHz
2. Standard configuration : 32 channels, 200kSPS/channel, 16 bit, differential, fixed bandwidth 130kHz
3. Software channel masking for higher sample rate, options:
  - 32 Channels Enabled, Fs = 200ksps
  - 16 Channels Enabled, Fs = 350ksps
4. Front end tolerates significant continuous overvoltage. Transient suppression is provided for VHDCI via transition panel eg BNC PANEL, see [Termination Panels](#).
5. Front panel connector: VHDCI or FFC (for local interconnect)
  - VHDCI compatible with D-TACQ range of termination panels
  - FFC compatible with 2xD37 front panel and facilitates custom transitions. Please contact [info@d-tacq.com](mailto:info@d-tacq.com) for details

### 1.1 Product Variants

- ACQ423ELF-32-200-16 32 channels, 200kSPS/ch 16 bit resolution with VHDCI Front Panel Connector
- ACQ423ELF-32-200-16-FFC 32 channels, 200kSPS/ch 16 bit resolution with FFC Connector. This is ordered in conjunction with custom front panel i.e D37

### 1.2 Carrier Compatibility

The FMC module standard adds user IO to carrier modules fitted with FPGA resource. D-TACQ recommends modules based on the Xilinx ZYNQ system on chip, combining FPGA resource with ARM CPU and Gigabit Ethernet see [Module Carriers](#).

The ELF module standard is a D-TACQ standard and is compatible with only D-TACQ Carriers.

Compatible carriers include:

- D-TACQ ACQ1001 : D-TACQ single site FMC/ELF carrier, Z7020
- D-TACQ ACQ1002 : D-TACQ dual site FMC/ELF carrier, Z7020
- D-TACQ ACQ2106 : D-TACQ 6 site ELF carrier, Z7030
- D-TACQ ACQ2206 : D-TACQ 6 site ELF carrier, Z7030
- D-TACQ ACQ1102 : D-TACQ 2 site FMC/ELF carrier, Z7030
- DAMC-FMC1Z7IO + D-TACQ ACQ400-MTCA-RTM-2 : 2 site ELF + 1 site FMC carrier, Z7030/7035
- Quantum Detectors PandABox, ZYNQ 7030 with single ELF site. Please contact [info@d-tacq.com](mailto:info@d-tacq.com) for details

D-TACQ supplies a complete working Intelligent Digitizer appliance including programmable logic and microprocessor system running Linux.

## 2 Physical

### 2.1 Board Outline

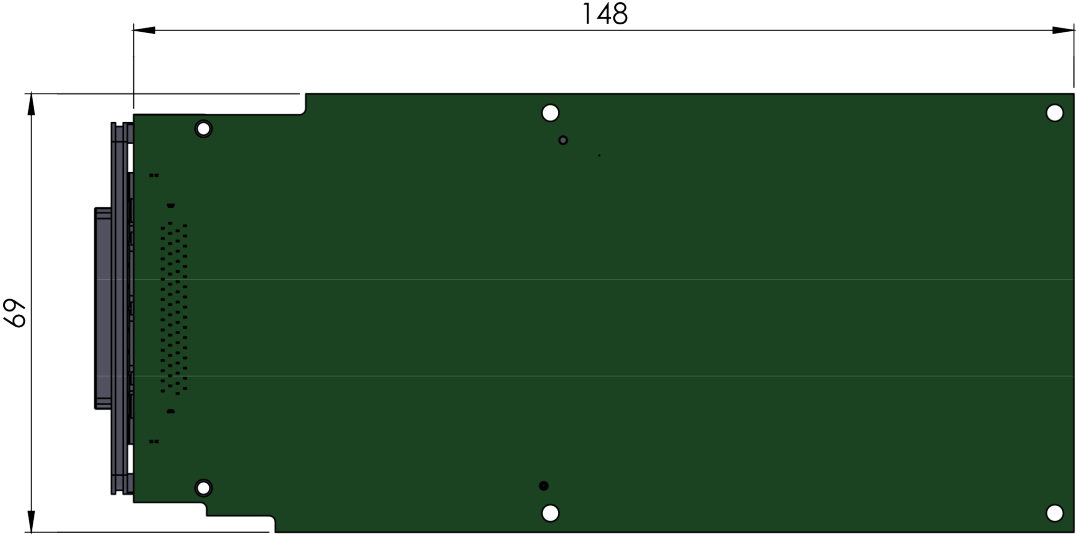


Figure 1: Board Outline D-TACQ ELF

### 2.2 Appearance with VHDCI Connector

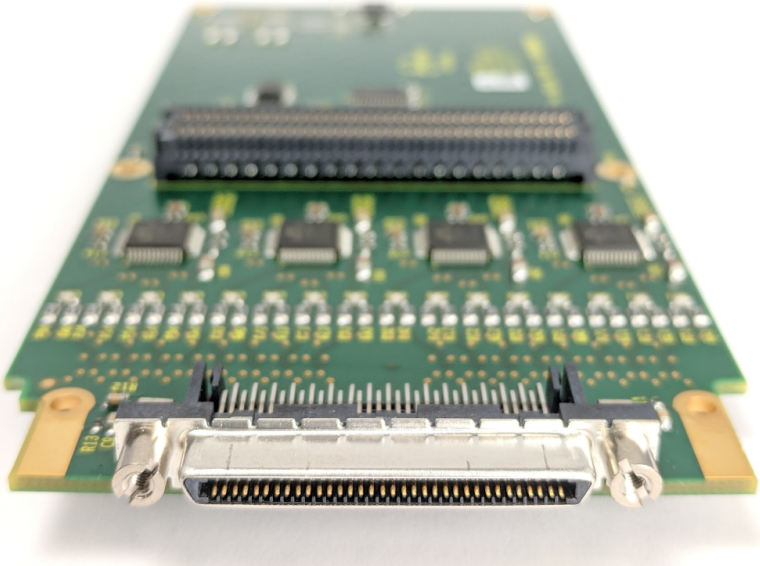


Figure 2: Board Photo

## 2.3 Front Panel Connectors

### 2.3.1 VHDCI

- 68 Pin VHDCI. Pinout compatible with D-TACQ BNCPANEL, SMAPANEL, LEMOPANEL, PTBPANEL
- For direct external cable to front panel

Pin	Function	Pin	Function
1	0V	35	0V
2	0V	36	0V
3	AI01+	37	AI01-
4	AI02+	38	AI02-
5	AI03+	39	AI03-
6	AI04+	40	AI04-
7	AI05+	41	AI05-
8	AI06+	42	AI06-
9	AI07+	43	AI07-
10	AI08+	44	AI08-
11	AI09+	45	AI09-
12	AI10+	46	AI10-
13	AI11+	47	AI11-
14	AI12+	48	AI12-
15	AI13+	49	AI13-
16	AI14+	50	AI14-
17	AI15+	51	AI15-
18	AI16+	52	AI16-
19	AI17+	53	AI17-
20	AI18+	54	AI18-
21	AI19+	55	AI19-
22	AI20+	56	AI20-
23	AI21+	57	AI21-
24	AI22+	58	AI22-
25	AI23+	59	AI23-
26	AI24+	60	AI24-
27	AI25+	61	AI25-
28	AI26+	62	AI26-
29	AI27+	63	AI27-
30	AI28+	64	AI28-
31	AI29+	65	AI29-
32	AI30+	66	AI30-
33	AI31+	67	AI31-
34	AI32+	68	AI32-

Table 1: Front Panel VHDCI Connector Pinout

### 2.3.2 Flexible Flat Cable - FFC

- For custom front panel, see below for an example. Please contact [info@d-tacq.com](mailto:info@d-tacq.com) for details

### 2.3.3 FFC to D37 Front Panel

The example below shows the FFC version fitted with a custom D37 Front panel. Note; there are two D37 connectors per mezzanine site.



Figure 3: Example Fitted to ACQ2106 Carrier, 96 channels in 1U



Figure 4: Front View of ACQ2106 Carrier, 96 channels in 1U

The pinout of the connectors on the D37 panel is given in the tables below@

Pin	Function	Pin	Function
1	AI01+	20	AI01-
2	AI02+	21	AI02-
3	AI03+	22	AI03-
4	AI04+	23	AI04-
5	AI05+	24	AI05-
6	AI06+	25	AI06-
7	AI07+	26	AI07-
8	AI08+	27	AI08-
9	AI09+	28	AI09-
10	AI10+	29	AI10-
11	AI11+	30	AI11-
12	AI12+	31	AI12-
13	AI13+	32	AI13-
14	AI14+	33	AI14-
15	AI15+	34	AI15-
16	AI16+	35	AI16-
17	0V		

Table 2: D37 Front Panel 1-16 Connector Pinout

Pin	Function	Pin	Function
1	AI17+	20	AI17-
2	AI18+	21	AI18-
3	AI19+	22	AI19-
4	AI20+	23	AI20-
5	AI21+	24	AI21-
6	AI22+	25	AI22-
7	AI23+	26	AI23-
8	AI24+	27	AI24-
9	AI25+	28	AI25-
10	AI26+	29	AI26-
11	AI27+	30	AI27-
12	AI28+	31	AI28-
13	AI29+	32	AI29-
14	AI30+	33	AI30-
15	AI31+	34	AI31-
16	AI32+	35	AI32-
17	0V		

Table 3: D37 Front Panel 17-32 Connector Pinout

### 3 Electrical Specification

#	Parameter	Value
1	Number of Channels	32
2	Sample Rate (Max)	200 kHz / 32 channels, 350 kHz / 16 channels, per channel simultaneous
3	Resolution	16-bit
4	Coupling	DC, Differential Input
5	Input Impedance	> 1 M $\Omega$
6	Input Voltage Range	$\pm 10V$ , $\pm 5V$ , 0-10V, 0-5.12V <sup>1</sup>
7	Input Voltage Withstand	$\pm 40V$ <sup>2</sup>
8	Offset Error	0.01% FS with numerical calibration
9	Gain Error	0.01% FS with numerical calibration
10	INL	$\pm 1$ LSB
10	DNL	$\pm 1$ LSB
11	Bandwidth(-3dB)	130kHz
12	CMRR	> 60 dB FS @ 1 kHz
13	Crosstalk	< 95 dB @ 1 kHz FS Input
14	THD	-90 dB <sup>3</sup>
15	SINAD	-84 dB <sup>3</sup>
16	SFDR	100 dBc <sup>3</sup>
17	SNR <sup>4</sup>	90 dB <sup>3</sup>
18	Temperature Stability	<25ppm/ $^{\circ}C$

<sup>1</sup> Input Full Scale may saturate below the Input Voltage Range span by up to 0.1%

<sup>2</sup> Maximum Continuous, up to  $\pm 100V$  transient

<sup>3</sup> Typical values measured at full scale with an 8.9 kHz input

<sup>4</sup>  $\pm 10V$  Input Range

Table 4: ACQ423ELF Electrical Performance

### 4 Mechanical & Environmental Specification

#	Parameter	Value
1	Form Factor	Long ELF
2	Power Consumption	Typical 2.5W, Max 3.5W
3	Environmental	0 $^{\circ}C$ - 50 $^{\circ}C$ Operational -10 $^{\circ}C$ - 85 $^{\circ}C$ Non-Operational
4	Mezzanine Socket	D-TACQ ELF Ultra Low Pin Count ULPC

Table 5: Mechanical & Environmental Specification

### Revision History

Revision	Date	Author(s)	Description
1	17/08/2018	JMcL	Initial Version
2	03/10/2019	JMcL	minor updates
3	07/10/2020	JMcL	Update to Single Ended Input Range
4	26/10/2023	JMcL	Updated carrier support
5	5/2/2024	SR	Addition of D37 pinout



#### Disclaimer

Specification subject to change without notice.

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