

# ACQ430FMC

8 Simultaneous Analog Input Module  
Developer Guide



## Product Developer Guide

- ACQ430FMC
- VITA-57, FMC-LPC Standard FMC Module
- 8 Channels of Simultaneous Analog input
- Up to 125kSPS/channel
- 24-bit resolution
- High SNR up to 108dB



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## 1 Product Variants

This module can be manufactured in the following versions:

- ACQ430FMC : 8 channels, FMC compliant, 36 way MDR (Mini-Centronics) Connector.
- ACQ430ELF : 8 channels, D-TACQ ELF compliant, 36 way MDR (Mini-Centronics) Connector.
- ACQ430FMC-4-LFP : 4 channels, FMC compliant , 4 single Pin LEMO connectors.
- ACQ430FMC-8-LFP : 8 channels, D-TACQ ELF compliant, 4 single Pin LEMO connectors on Front Panel, 4 single Pin LEMO connectors on Top Deck.

Please contact [info@d-tacq.com](mailto:info@d-tacq.com) for other Front Panel connection options.

## 2 Front Panel Connectors

### 2.1 Front Panel 36 Pin MDR (Mini-Centronics) Connector

- 36 Pin MDR (Mini-Centronics) 3M 10236-55G3PL.
- Mating Part 3M 10136-6000EL.
- Pinout compatible with D-TACQ DIN RAIL ACQ430-TERM03 Panel For direct external cable to front panel.

Pin	Function	Pin	Function
1	0V	19	0V
2	CH_08+	20	CH_08-
3	0V	21	0V
4	CH_07+	22	CH_07+
5	+12V	23	+5V
6	TRIG	24	CLK
7	0V	25	0V
8	CH_06+	26	CH_06-
9	0V	27	0V
10	CH_05+	28	CH_05-
11	0V	29	0V
12	CH_04+	30	CH_04-
13	0V	31	0V
14	CH_03+	32	CH_03-
15	0V	33	0V
16	CH_02+	34	CH_02-
17	0V	35	0V
18	CH_01+	36	CH_01-

Table 1: Front Panel MDR 36 Connector Pinout

### 2.2 Single Pin LEMO

- Single-pin LEMO 00 Series Mini Coax connector (part EPL.00.250.NTN).
- Mating Part FFA.00.250.NTAC29.

Pin	Function	Pin	Function
Centre	CHANNEL +ve	Shell	CHANNEL -ve

Table 2: Front Panel LEMO Connectors Pinout

### 3 Main Front End and ADC Devices

There are 8 identical sets of Front End Amplification and 1 8channel ADC devices as follows:

The signals are received by a differential amplifier configuration consisting of Texas Instruments [OPA4209](#) unity gain buffers and a Texas instruments Differential Amplifier [THS4522](#).

The ACQ430FMC uses the Texas Instruments [ADS1278](#) 24 bit ADC, please review the data-sheet for using this device.

### 4 I<sup>2</sup>C Devices

The module is fitted with 2 I<sup>2</sup>C devices as follows:

Address	Device	Description
0x28	AD7417	Temperature Sensor and Analog Input
0x54	M24C64	Serial IPMI FRU PROM

Table 3: I<sup>2</sup>C devices

#### 4.1 AD7417 Temperature Sensor

See the data sheet at [AD7417](#)

The AD7417 also monitors key power supply values to verify correct operation. Most OS drivers for the AD7417 device output in the default voltage level of the device of 0-2.5V. The correct output of the voltage monitor can be calculated as per the following table:

Input	Voltage Rail	Input Conversion
1	-15V <sub>analogue</sub>	Voltage = (ADC Reading x 2.3) - ( Channel 2 Calculated Voltage x 1.3)
2	+15V <sub>analogue</sub>	Voltage = ADC Reading x 11
3	+5V <sub>analogue</sub>	Voltage = ADC Reading x 3
4	+1.8V	Voltage = ADC Reading x 1.1

Table 4: AD7417 Voltage Calculations

#### 4.2 Serial IPMI FRU PROM

This is a standard FMC FRU devices the contents of the PROM are as per the FMC standard and the *IPMI Platform Management FRU Information Storage Definition v1.0*.

Below is an example of a ACQ430FMC module with the serial number 16:

```
fru-dump -b F43010016.fru
read 231 bytes from F43010016.fru
Date of Man      : Thu Mar 31 12:37:00 2016
Manufacturer    : D-TACQ Solutions
Product Name    : ACQ430FMC
Serial Number   : F43010016
Part Number     : ACQ430FMC-8-LFP N=8 M=03
FRU File ID    : 2016-03-31 11:37:29.740743
```

D-TACQ uses the Part number field with 2 additional entries.

N=8 This is used to indicate that the module has 8 channels.

M=03 This is used for the FPGA logic to indicate the module type ACQ430FMC.

## 5 FMC Connector Pinout

Pin	Signal Name	Description
p_FMC_CLK0_M2C_p	EXT_CLK	External Clock
p_FMC_CLK0_M2C_n	Not Used	Not Used
p_FMC_LA00_CC_p	ADC_MODE_0	ADC_MODE_0
p_FMC_LA00_CC_n	Not Used	Not Used
p_FMC_LA01_CC_p	Not Used	Not Used
p_FMC_LA01_CC_n	Not Used	Not Used
p_FMC_LA02_p	FP_SCL	Optional I2C Bus SCL (MDR 36 Only)
p_FMC_LA02_n	Not Used	Not Used
p_FMC_LA03_p	FP_SDA	Optional I2C Bus SDA (MDR 36 Only)
p_FMC_LA03_n	Not Used	Not Used
p_FMC_LA04_p	ADC_FSYNC	ADC_FSYNC
p_FMC_LA04_n	Not Used	Not Used
p_FMC_LA05_p	RIBBON_PRSENT_n	TOP Deck Ribbon Present (LPC Only)
p_FMC_LA05_n	Not Used	Not Used
p_FMC_LA06_p	Not Used	Not Used
p_FMC_LA06_n	Not Used	Not Used
p_FMC_LA07_p	Not Used	Not Used
p_FMC_LA07_n	Not Used	Not Used
p_FMC_LA08_p	ADC_SPI_CLK	ADC SPI Clock
p_FMC_LA08_n	Not Used	Not Used
p_FMC_LA09_p	Not Used	Not Used
p_FMC_LA09_n	Not Used	Not Used
p_FMC_LA10_p	CLOCK_DIR	Set the Direction of the Clock Pin
p_FMC_LA10_n	Not Used	Not Used
p_FMC_LA11_p	Not Used	Not Used
p_FMC_LA11_n	Not Used	Not Used
p_FMC_LA12_p	ADC_SDO	ADC SDO Data Output
p_FMC_LA13_p	EXT_TRIG	External Trigger
p_FMC_LA14_p	TRIGGER_DIR	Set Trigger In or Out (MDR 36 Only)
p_FMC_LA15_p	Not Used	Not Used
p_FMC_LA16_p	ADC_SYNC_n	ADC SYNC Pin
p_FMC_LA17_CC_p	Not Used	Not Used
p_FMC_LA18_CC_p	Not Used	Not Used
p_FMC_LA19_p	Not Used	Not Used
p_FMC_LA20_p	Not Used	Not Used
p_FMC_LA21_p	Not Used	Not Used
p_FMC_LA22_p	Not Used	Not Used
p_FMC_LA23_p	Not Used	Not Used

Table 5: Mezzanine Connector Pinout

## 6 VHDL Top Level Template

The sample code below gives a prototype VHDL entity declaration for the FMC I/O pins of the mezzanine. The pin naming convention on the module is as per the FMC specification.

```

-----
--                               ACQ430FMC Zynq Project Top Level of Module Connection
-----
--! Standard Libraries - numeric.std for all designs
library ieee;
use ieee.std_logic_1164.all;      -- Standard Logic Functions
use ieee.numeric_std.all;        -- Numeric Functions for Signed / Unsigned Arithmetic

--! Xilinx Primitive Library
library UNISIM;
use UNISIM.VComponents.all;     -- Xilinx Primitives

--! Top Level of the ACQ430FMC Module
entity ACQ430FMC_TOP is
port(
-----
-- External I/O hooks --
-----
p_FMC_CLK0_M2C_p      : inout  std_logic;    --! EXT_CLK
p_FMC_CLK0_M2C_n      : inout  std_logic;    --! Not Used
p_FMC_LA00_CC_p       : inout  std_logic;    --! ADC_MODE_0
p_FMC_LA00_CC_n       : inout  std_logic;    --! Not Used
p_FMC_LA01_CC_p       : inout  std_logic;    --! Not Used
p_FMC_LA01_CC_n       : inout  std_logic;    --! Not Used
p_FMC_LA02_p          : inout  std_logic;    --! FP_SCL
p_FMC_LA02_n          : inout  std_logic;    --! Not Used
p_FMC_LA03_p          : inout  std_logic;    --! FP_SDA
p_FMC_LA03_n          : inout  std_logic;    --! Not Used
p_FMC_LA04_p          : inout  std_logic;    --! ADC_FSYNC
p_FMC_LA05_p          : inout  std_logic;    --! TOP Deck Present - JWM to be added
p_FMC_LA06_p          : inout  std_logic;    --! Not Used
p_FMC_LA07_p          : inout  std_logic;    --! Not Used
p_FMC_LA08_p          : inout  std_logic;    --! ADC_SPI_CLK
p_FMC_LA09_p          : inout  std_logic;    --! Not Used
p_FMC_LA10_p          : inout  std_logic;    --! CLOCK_DIR
p_FMC_LA11_p          : inout  std_logic;    --! Not Used
p_FMC_LA12_p          : inout  std_logic;    --! ADC_SDO
p_FMC_LA13_p          : inout  std_logic;    --! EXT_TRIG
p_FMC_LA14_p          : inout  std_logic;    --! TRIGGER_DIR
p_FMC_LA15_p          : inout  std_logic;    --! Not Used
p_FMC_LA16_p          : inout  std_logic;    --! ADC_SYNC_n
p_FMC_LA17_CC_p       : inout  std_logic;    --! Not Used
p_FMC_LA18_CC_p       : inout  std_logic;    --! Not Used
p_FMC_LA19_p          : inout  std_logic;    --! Not Used
p_FMC_LA20_p          : inout  std_logic;    --! Not Used
p_FMC_LA21_p          : inout  std_logic;    --! Not Used
p_FMC_LA22_p          : inout  std_logic;    --! Not Used
p_FMC_LA23_p          : inout  std_logic;    --! Not Used
);
end ACQ430FMC_TOP;

```

The ACQ430FMC module connects ADC\_MODE\_0 for mode control on the ADC supporting the following modes.

- ADC\_MODE\_0 = 0, High Speed
- ADC\_MODE\_0 = 1, High Resolution

## Revision History

Revision	Date	Author(s)	Description
1	February 2025	JMcL	First Release



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