DIO422FMC Product Specification

High Performance Simultaneous Data Acquisition

Contents

Revision History

Revision	Date	Author(s)	Description
1.0	17/08/2023	SR	Created

Glossary

- FMC : VITA57.1 FPGA Mezzanine Card
- ELF : Electrically Extended FMC, implies ULPC or DULPC (only compatible with D-TACQ carriers)
- LPC : FMC Low Pin Count standard as per VITA57.1
- ULPC : Subset by D-TACQ, Ultra Low Pin Count
- DULPC : Subset by D-TACQ, Differential Ultra Low Pin Count (ULPC with extra differential signalling)
- Xilinx ZYNQ System on Chip (SoC)
- FPGA : Field Programmable Gate Array

1 Product Description

- DIO422FMC is a Quadrature Encoder module
- Capable of receiving standard A/B Quadrature signals with additional INDEX and ERROR signals
- Up to 12.5 MHz edge rate on each input, (40 ns HIGH time), resulting in possible 50 MHz quadrature counter
- RS422 I/O on D15 connector

1.1 Product Variants

- DIO422FMC
- DIO422ELF
- DIO422ELF-STIM : Stimulator variant with driver capability for stimulating the standard product inputs

1.2 Applications

- Quadrature Encoders

1.3 Carrier Compatibility

The FMC module standard adds user IO to carrier modules fitted with FPGA resource. D-TACQ recommends modules based on the Xilinx ZYNQ system on chip, combining FPGA resource with ARM CPU and Gigabit Ethernet.

The ELF module standard is a D-TACQ standard and is compatible with only D-TACQ Carriers.

Compatible carriers include:

- D-TACQ ACQ1001 : D-TACQ single slot FMC carrier, Z7020
- D-TACQ ACQ1002 : D-TACQ dual slot FMC carrier, Z7020
- D-TACQ ACQ2106 : D-TACQ 6 slot FMC carrier, Z7030
- D-TACQ ACQ2206 : D-TACQ 6 slot FMC carrier, Z7030
- D-TACQ ACQ1102 : D-TACQ 2 slot FMC carrier, Z7030
- DAMC-FMC1Z7IO + D-TACQ ACQ400-MTCA-RTM-2

D-TACQ supplies a complete working Intelligent Digitizer appliance including programmable logic and microprocessor system running Linux.

2 Physical

2.1 Board Outline

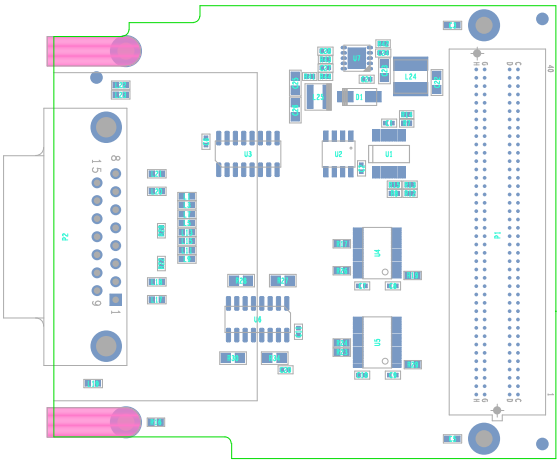

Figure 1: Board Outline

2.2 Appearance

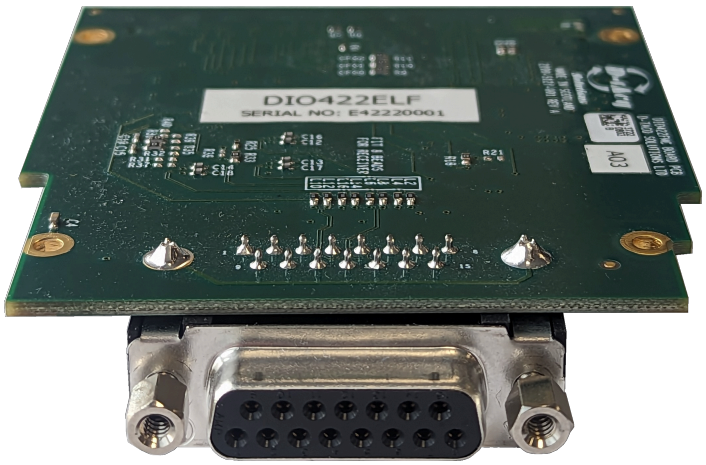

Figure 2: Board Appearance

2.3 Front Panel Connectors & Pinout

- D Sub Connector DB15 (TE 5747845-4)
- Receives RS422 inputs

Pin	Signal Name	Description
1	SETUP	(Optional) Setup
2	0VD	0V Digital
3	E-	Error (E) Complement
4	Z-	Index (Z) Complement
5	B-	B Complement
6	A-	A Complement
7	NC	Not Used
8	NC	Not Used
9	0VD	0V Digital
10	RES_Q	Not Used
11	E+_P	Error (E) or Single-ended P
12	Z+	Index (Z)
13	B+	B
14	A+	A
15	NC	Not Used

Table 1: Front Panel D15 Connector Pinout

3 Electrical Specification

#	Parameter	Value
1	AquadB Channels	1
2	Max AquadB Count Rate	50 MHz
3	Input Signals	RS-422
4	Maximum Input Frequency	12.5 MHz

Table 2: PRODUCTNAMEHERE Electrical Performance

3.1 Signal Timing AquadB Signal Reception

Quadrature signals should have a minimum pulse width as shown below:

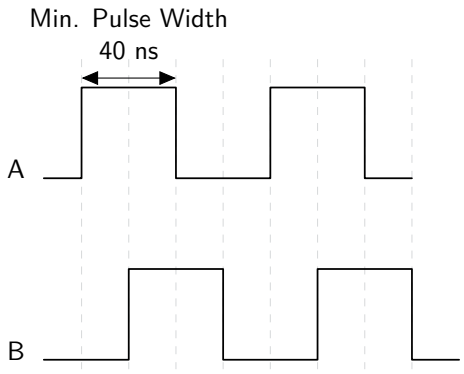

Figure 3: AquadB signals and minimum pulse width

In other words, a maximum input frequency on each A or B signal of 12.5 MHz.
This results in a quadrature count rate of 4 $\times$ 12.5 MHz = 50 MHz

4 Mechanical & Environmental Specification

#	Parameter	Value
1	Form Factor	Standard FMC
2	Power Source	DC 12V, XXX mA DC 3.3V, XXX mA
3	Environmental	0 °C - 50 °C Operational −10 °C - 85 °C Non-Operational
4	Mezzanine Socket	Standard FMC, Low Pin Count LPC

Table 3: Mechanical & Environmental Specification

A FMC Information

A.1 I²C Devices

The board is fitted with 2 I²C devices as follows

Address	Device	Description
0x28	AD7417	Temperature Sensor and Analog Input
0x50	M24C64	Serial IPMI FRU PROM

Table 4: I²C devices

A.1.1 AD7417 Temperature Sensor

See the data sheet at AD7417

A.1.2 Serial IPMI FRU PROM

This is a standard FMC FRU devices the contents of the PROM are as per the FMC standard and the *IPMI Platform Management FRU Information Storage Definition v1.0*

Below is an example of a DIO422FMC module with the serial number 10.

```
./fru-dump fru/E42220010.fru
header 0x6cf010 bia 0x6cf018
fru/E42220010.fru: manufacturer: D-TACQ Solutions
header 0x6cf010 bia 0x6cf018
fru/E42220010.fru: product-name: DIO422ELF
header 0x6cf010 bia 0x6cf018
fru/E42220010.fru: serial-number: E42220010
header 0x6cf010 bia 0x6cf018
fru/E42220010.fru: part-number: DIO422ELF N=4 M=71
```

A.2 FMC Connector Pinout

Pin	Signal Name	Description
p_FMC_CLK0_M2C_p	-	Not Used
p_FMC_CLK0_M2C_n	-	Not Used
p_FMC_CLK1_C2M_p	-	Not Used
p_FMC_CLK1_C2M_n	-	Not Used
p_FMC_LA00_CC_p	FMC_QUAD_A_Rx	Not Used
p_FMC_LA00_CC_n	-	Not Used
p_FMC_LA01_CC_p	FMC_QUAD_B_Rx	Not Used
p_FMC_LA01_CC_n	-	Not Used
p_FMC_LA02_p	FMC_QUAD_Z_Rx	Not Used
p_FMC_LA02_n	-	Not Used
p_FMC_LA03_p	FMC_QUAD_E_Rx	Not Used
p_FMC_LA03_n	-	Not Used
p_FMC_LA04_p	FMC_ENC_RES_Q_Rx	Not Used
p_FMC_LA04_n	-	Not Used
p_FMC_LA05_p	FMC_ENC_P_Rx	Not Used
p_FMC_LA05_n	-	Not Used
p_FMC_LA06_p	-	Not Used
p_FMC_LA06_n	-	Not Used
p_FMC_LA07_p	FMC_QUAD_A_Tx	Not Used
p_FMC_LA07_n	-	Not Used
p_FMC_LA08_p	FMC_QUAD_B_Tx	Not Used
p_FMC_LA08_n	-	Not Used
p_FMC_LA09_p	FMC_QUAD_Z_Tx	Not Used
p_FMC_LA09_n	-	Not Used
p_FMC_LA10_p	FMC_QUAD_E_Tx	Not Used
p_FMC_LA10_n	-	Not Used
p_FMC_LA11_p	FMC_ENC_RES_Q_Tx	Not Used
p_FMC_LA11_n	-	Not Used
p_FMC_LA12_p	RS485_Tx_EN	Not Used
p_FMC_LA13_p	RS485_Tx_EN_n	Not Used
p_FMC_LA14_p	DIO_EN_n	Not Used
p_FMC_LA15_p	CONFIG0	Not Used
p_FMC_LA16_p	CONFIG1	Not Used
p_FMC_LA17_CC_p	-	Not Used
p_FMC_LA18_CC_p	-	Not Used
p_FMC_LA19_p	-	Not Used
p_FMC_LA20_p	-	Not Used
p_FMC_LA21_p	-	Not Used
p_FMC_LA22_p	-	Not Used
p_FMC_LA23_p	-	Not Used

Table 5: Mezzanine Connector Pinout

B VHDL Top Level Template

The sample code below gives a prototype VHDL entity declaration for the FMC I/O pins of the mezzanine. The pin naming convention on the module is as per the FMC specification.

```
----------------------------------------------------------------------------------
--        ACQ420FMC I/Os
----------------------------------------------------------------------------------



--! Standard Libraries - numeric.std for all designs
library ieee;
use ieee.std_logic_1164.all;    -- Standard Logic Functions
use ieee.numeric_std.all;   -- Numeric Functions for Signed / Unsigned Arithmetic

--! Xilinx Primitive Library
library UNISIM;
use UNISIM.VComponents.all;   -- Xilinx Primitives

entity DIO422FMC_TOP is
port(
  p_FMC_CLK0_M2C_p    : inout std_logic;          --!
  p_FMC_CLK0_M2C_n    : inout std_logic;          --!
  p_FMC_LA00_CC_p     : inout std_logic;          --! FMC_QUAD_A_Rx
  p_FMC_LA00_CC_n     : inout std_logic;          --!
  p_FMC_LA01_CC_p     : inout std_logic;          --! FMC_QUAD_B_Rx
  p_FMC_LA01_CC_n     : inout std_logic;          --!
  p_FMC_LA02_p      : inout std_logic;          --! FMC_QUAD_Z_Rx
  p_FMC_LA02_n      : inout std_logic;          --!
  p_FMC_LA03_p      : inout std_logic;          --! FMC_QUAD_E_Rx
  p_FMC_LA03_n      : inout std_logic;          --!
  p_FMC_LA04_p      : inout std_logic;          --! FMC_ENC_RES_Q_Rx
  p_FMC_LA04_n      : inout std_logic;          --!
  p_FMC_LA05_p      : inout std_logic;          --! FMC_ENC_P_Rx
  p_FMC_LA05_n      : inout std_logic;          --!
  p_FMC_LA06_p      : inout std_logic;          --!
  p_FMC_LA06_n      : inout std_logic;          --!
  p_FMC_LA07_p      : inout std_logic;          --! FMC_QUAD_A_Tx
  p_FMC_LA07_n      : inout std_logic;          --!
  p_FMC_LA08_p      : inout std_logic;          --! FMC_QUAD_B_Tx
  p_FMC_LA08_n      : inout std_logic;          --!
  p_FMC_LA09_p      : inout std_logic;          --! FMC_QUAD_Z_Tx
  p_FMC_LA09_n      : inout std_logic;          --!
  p_FMC_LA10_p      : inout std_logic;          --! FMC_QUAD_E_Tx
  p_FMC_LA10_n      : inout std_logic;          --!
  p_FMC_LA11_p      : inout std_logic;          --! FMC_ENC_RES_Q_Tx
  p_FMC_LA11_n      : inout std_logic;          --!
  p_FMC_LA12_p      : inout std_logic;          --! RS485_Tx_EN
  p_FMC_LA13_p      : inout std_logic;          --! RS485_Tx_EN_n
  p_FMC_LA14_p      : inout std_logic;          --! DIO_EN_n
  p_FMC_LA15_p      : inout std_logic;          --! CONFIG0
  p_FMC_LA16_p      : inout std_logic;          --! CONFIG1
  p_FMC_LA17_CC_p     : inout std_logic;          --! CONFIG2
  p_FMC_LA18_CC_p     : inout std_logic;          --!
  p_FMC_LA19_p      : inout std_logic;          --!
  p_FMC_LA20_p      : inout std_logic;          --!
  p_FMC_LA21_p      : inout std_logic;          --!
  p_FMC_LA22_p      : inout std_logic;          --!
  p_FMC_LA23_p      : inout std_logic         --!

  );
end DIO422FMC_TOP;
```

The internal names on the comments have the following definitions

```
----------------------------------------------------------------------------------
-- FMC pin name translation signals.
----------------------------------------------------------------------------------
--Inputs
signal  p_QUAD_A_Rx   : std_logic         := '0';
signal  p_QUAD_B_Rx   : std_logic         := '0';
signal  p_QUAD_Z_Rx   : std_logic         := '0';
signal  p_QUAD_E_Rx   : std_logic         := '0';
signal  p_ENC_RES_Q_Rx  : std_logic         := '0';
signal  p_ENC_P_Rx    : std_logic         := '0';

signal  p_CONFIG0   : std_logic         := '0';
signal  p_CONFIG1   : std_logic         := '0';
signal  p_CONFIG2   : std_logic         := '0';


--Outputs (for Stimulator test module)
signal  p_QUAD_A_Tx   : std_logic         := '0';
signal  p_QUAD_B_Tx   : std_logic         := '0';
signal  p_QUAD_Z_Tx   : std_logic         := '0';
signal  p_QUAD_E_Tx   : std_logic         := '0';
signal  p_ENC_RES_Q_Tx  : std_logic         := '0';
signal  p_RS485_Tx_EN : std_logic         := '0';
signal  p_RS485_Tx_EN_n : std_logic         := '0';
signal  p_DIO_EN_n    : std_logic         := '0';
```