



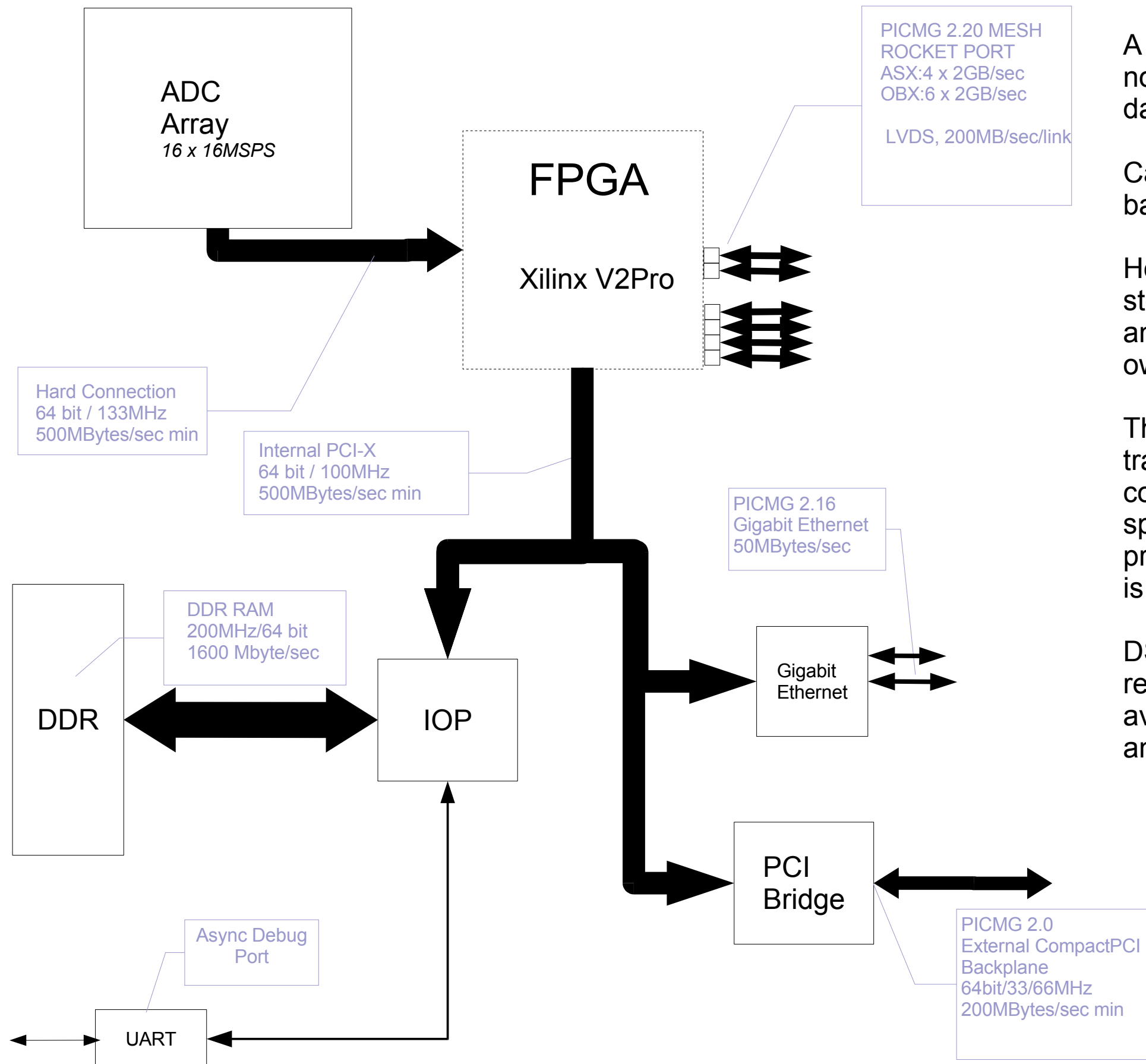
Embedded Signal Processing Enhances Data Acquisition

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ACQ216CPCI Simultaneous Digitizer Architecture

Capture One Gigabyte Data in 2s



A modern digitizer like ACQ216CPCI has no problem capturing vast amounts of data.

Capturing and viewing raw data is a basic function of the device.

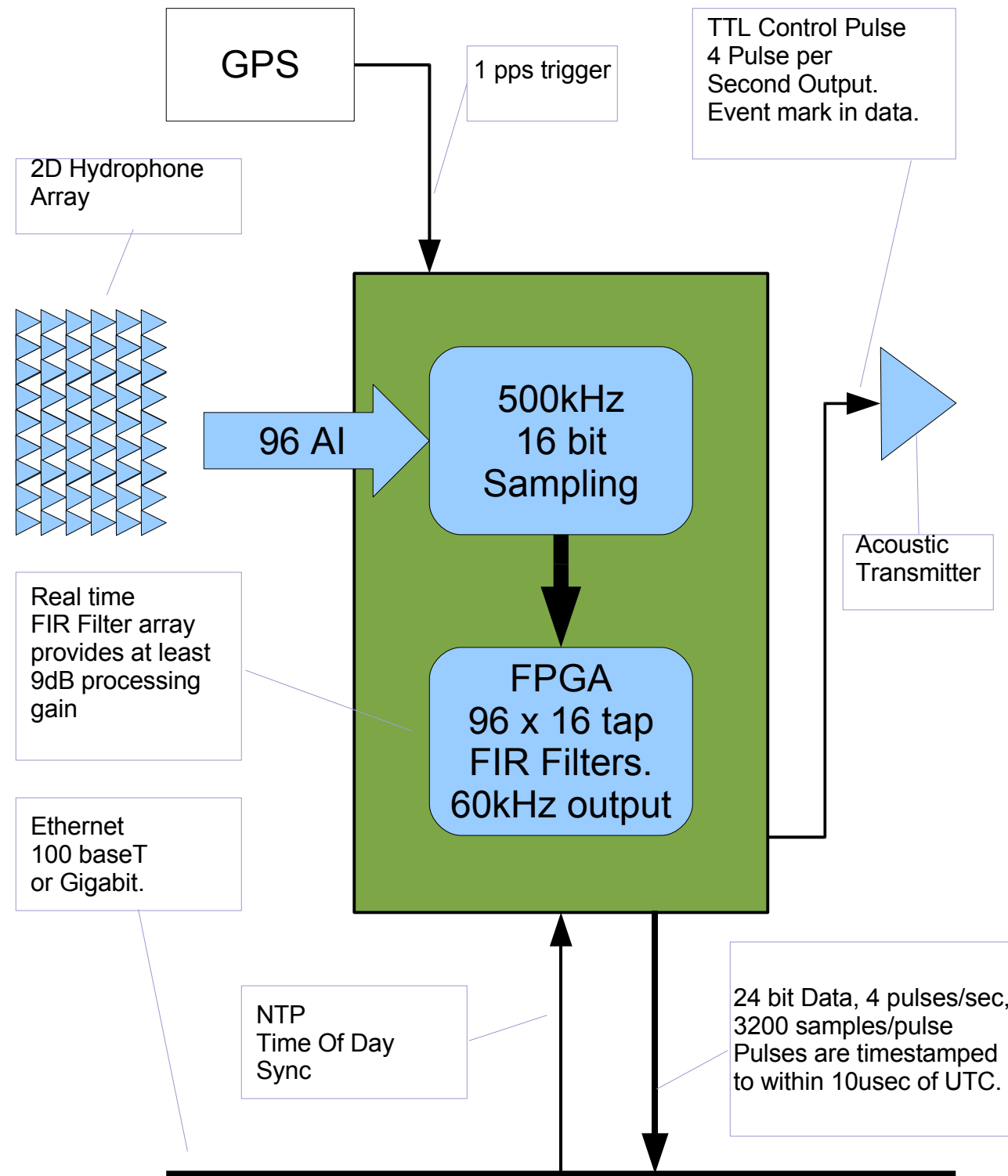
However the time to upload the data, storage of this data, and performing later analysis are all challenging problems owing to the sheer volume of data.

The primary function of the FPGA is data transfer, however it can also be configured as a powerful “application specific computer”. Combined with the programmable local microprocessor, this is a very flexible solution.

DSP algorithms may be applied simply to reduce data, or to make processed data available rapidly, or for real time control and protection.

ACQ196CPCI Seismic Survey Application

Pulsed Streaming Data with Oversampling



ACQ196CPCI uses a Xilinx Spartan 3 FPGA.

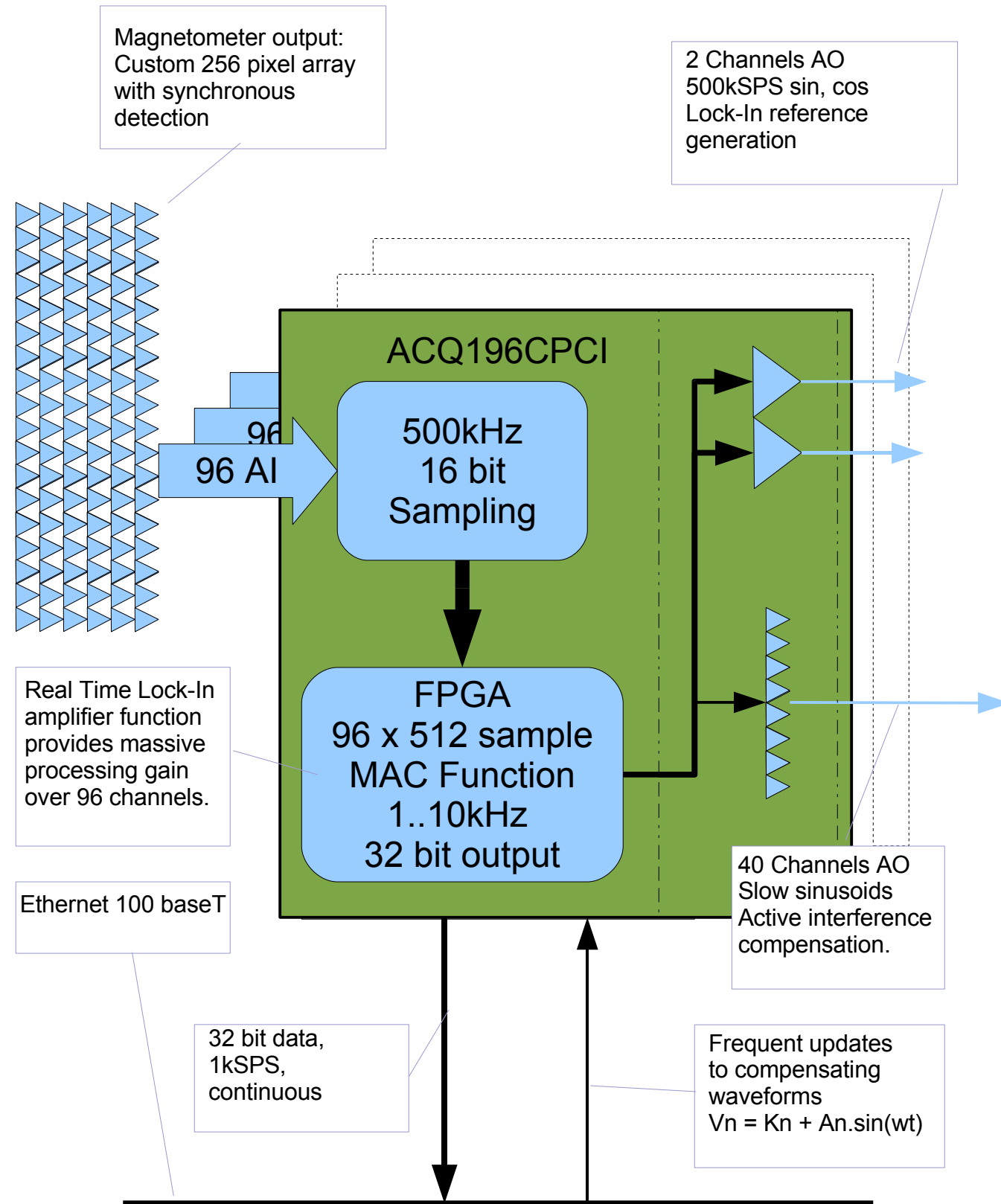
Custom DSP firmware has been implemented to provide a FIR function, processing the input data in real time, and providing a reduced-rate, decimated output.

FIR Filtering adds processing gain to Sonar application.

The FIR filter firmware can be used for noise reduction in any appropriate application.

ACQ196CPCI Medical Imaging Application

Continuous Streaming Data with DSP Lock In Detection



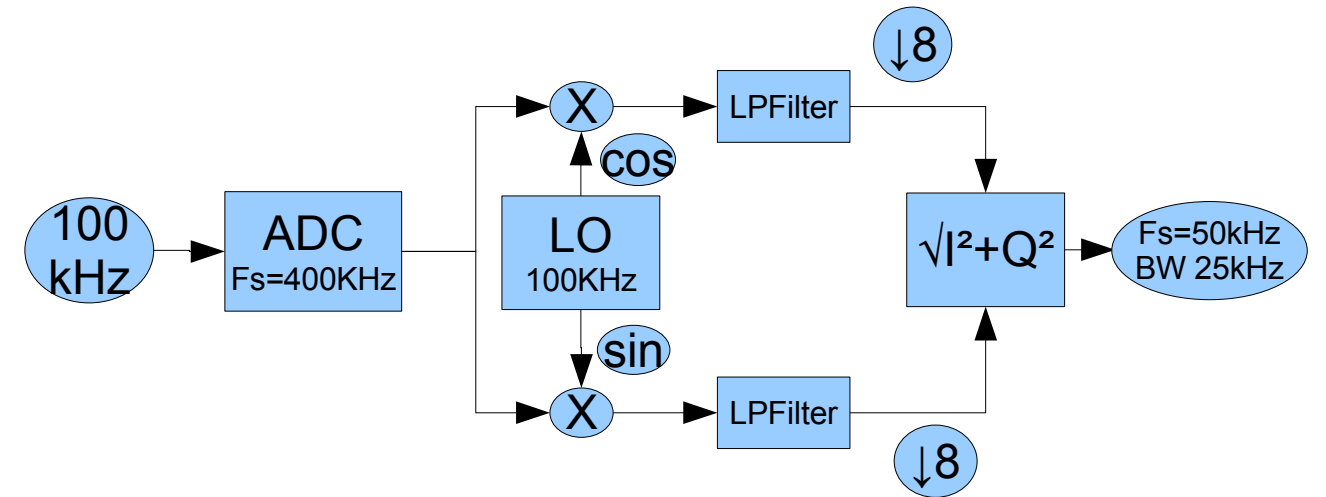
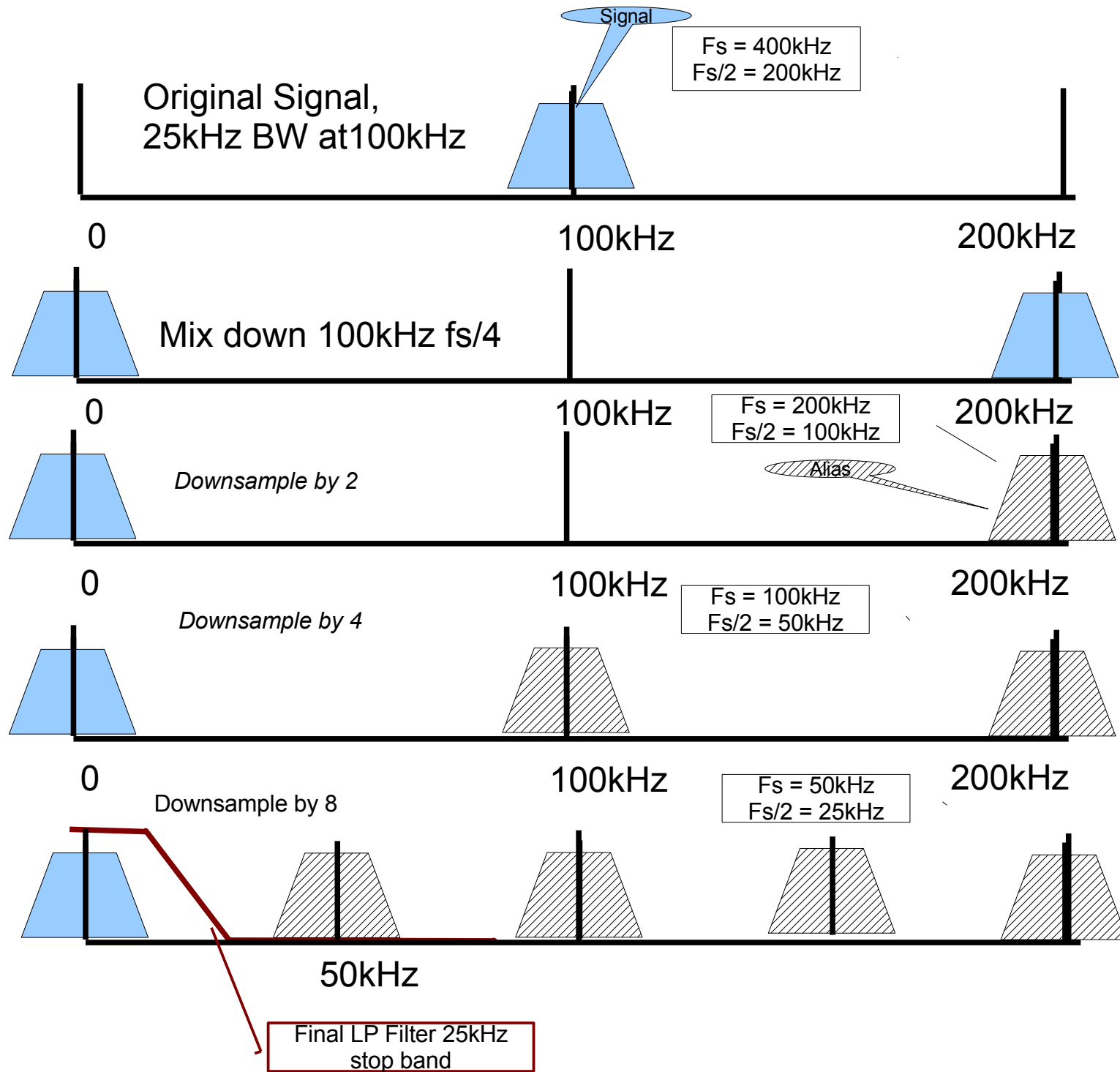
96 channel digital Lock-in amplifier provides massive SNR improvement to medical imaging application

In this case, the circuit generates its own reference signal for output to the system, but it's equally possible to pick up an external reference on an input channel.

A possible fusion application for this technology is to record and demodulate the output of a Photo Elastic Multiplexer, for example in a Motional Stark Effect diagnostic.

96 channel Digital Downconverter

Extract base band signal from carrier, reduce output data size



This solution is for an ultrasound application.

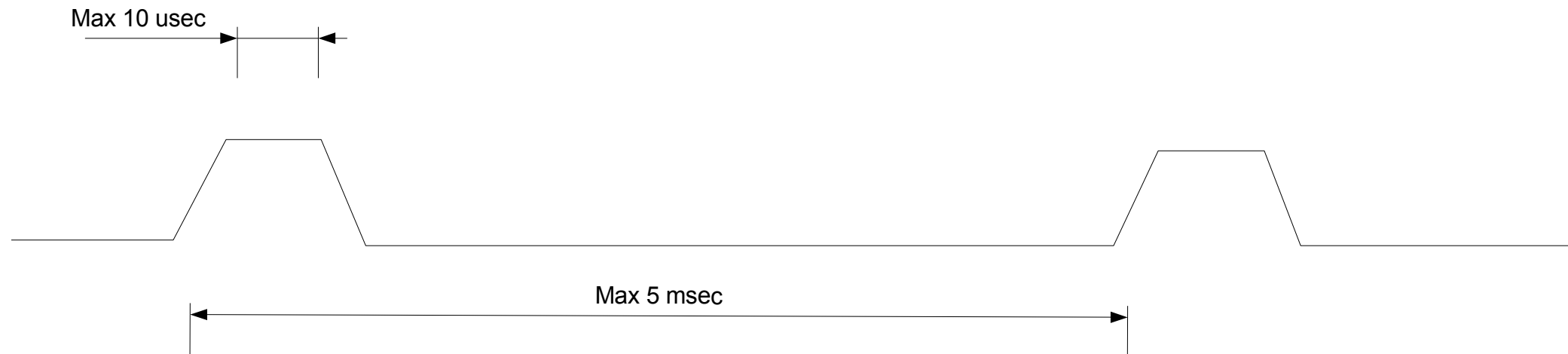
Implemented on 96 channels on ACQ196CPCI, 25kHz signal on a 100kHz carrier is mixed down to base band, and, after decimation, an 8 fold data reduction is achieved.

The same principle could easily be applied to RF.

Eg: 16 channels on ACQ216CPCI, 1MHz signal on a 16MHz carrier, output data rate after mix and decimation is 2MS/s.

Thompson Scattering Example

Threshold detection reduces huge data set to duration of each laser pulse.



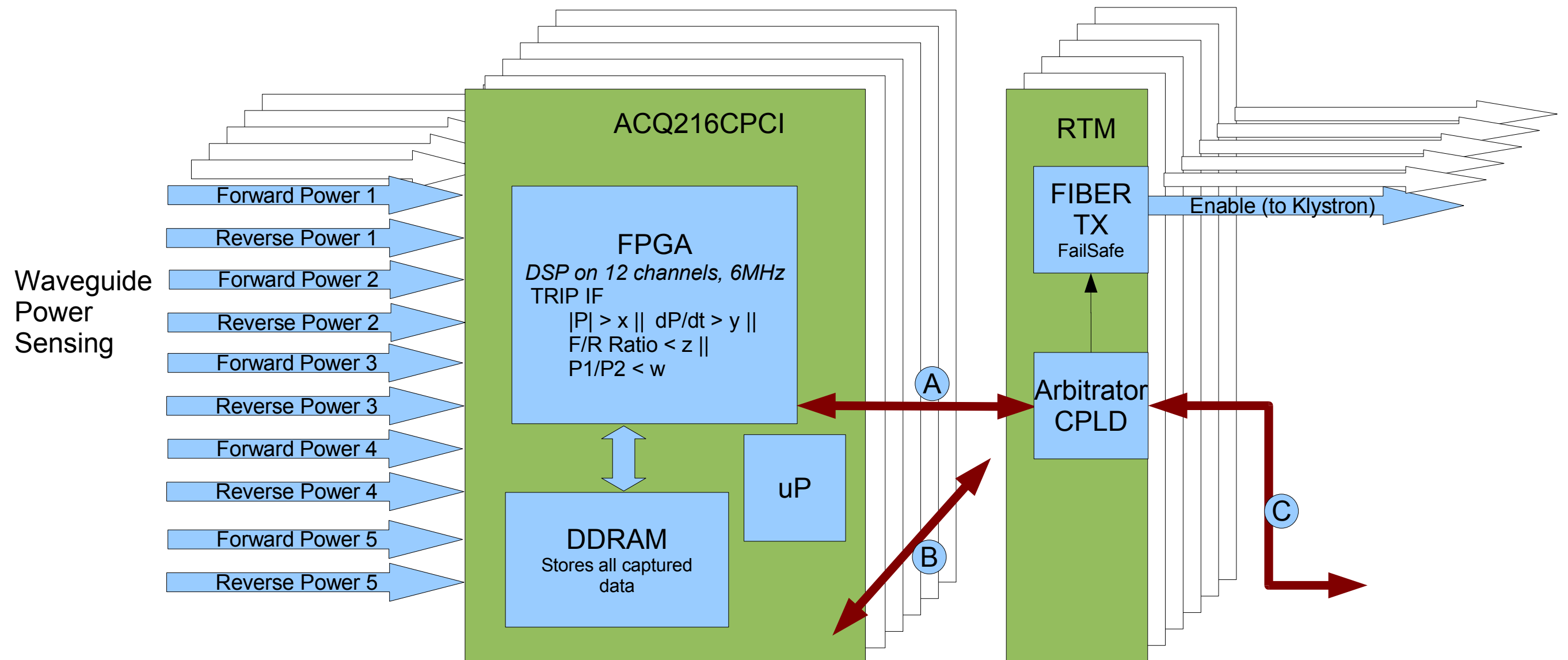
- Several hundred capture channels, 500kS/s. Shot duration 5s, total data set > 500K bytes
- Data is only of interest during laser pulse, pulses are 10usec duration, with “random” spacing.
- Laser is rated at 400pulses per second.
- The duty cycle of the data is only 4:1000

Solution:

- ACQ196CPCI captures data to memory at full rate.
- Laser pulse is configured as an Event input – FPGA samples, and a table of event vs approximate sample number is recorded.
- Post shot, embedded microprocessor firmware uses the event table to seed a pulse search algorithm. Each identified pulse is placed in a virtual file, ready for upload to data archive system. Data transfer by FTP or embedded MDSplus client.
- The Post shot search is very rapid, data is available for upload within 5s.
- The data upload size is reduced by factor 250, and each pulse is timestamped.
- The full data set is still available for cross check, if required.

Coupler Protection System

RF signals, real time signal processing, thresholding and safety interlock.



Tokamak Microwave Heating System comprises 12 Klystrons and a “jungle gym” waveguide power delivery mechanism.

For each Klystron, Forward and Reverse Power is measured at 5 points in the waveguide.

The Protection System monitors the signals, performing absolute and ratiometric measurements against stored thresholds to generate a trip signal.

The protection system comprises 12 ACQ216CPCI digitizers, 6 in each of two 8 slot Compact PCI crates.

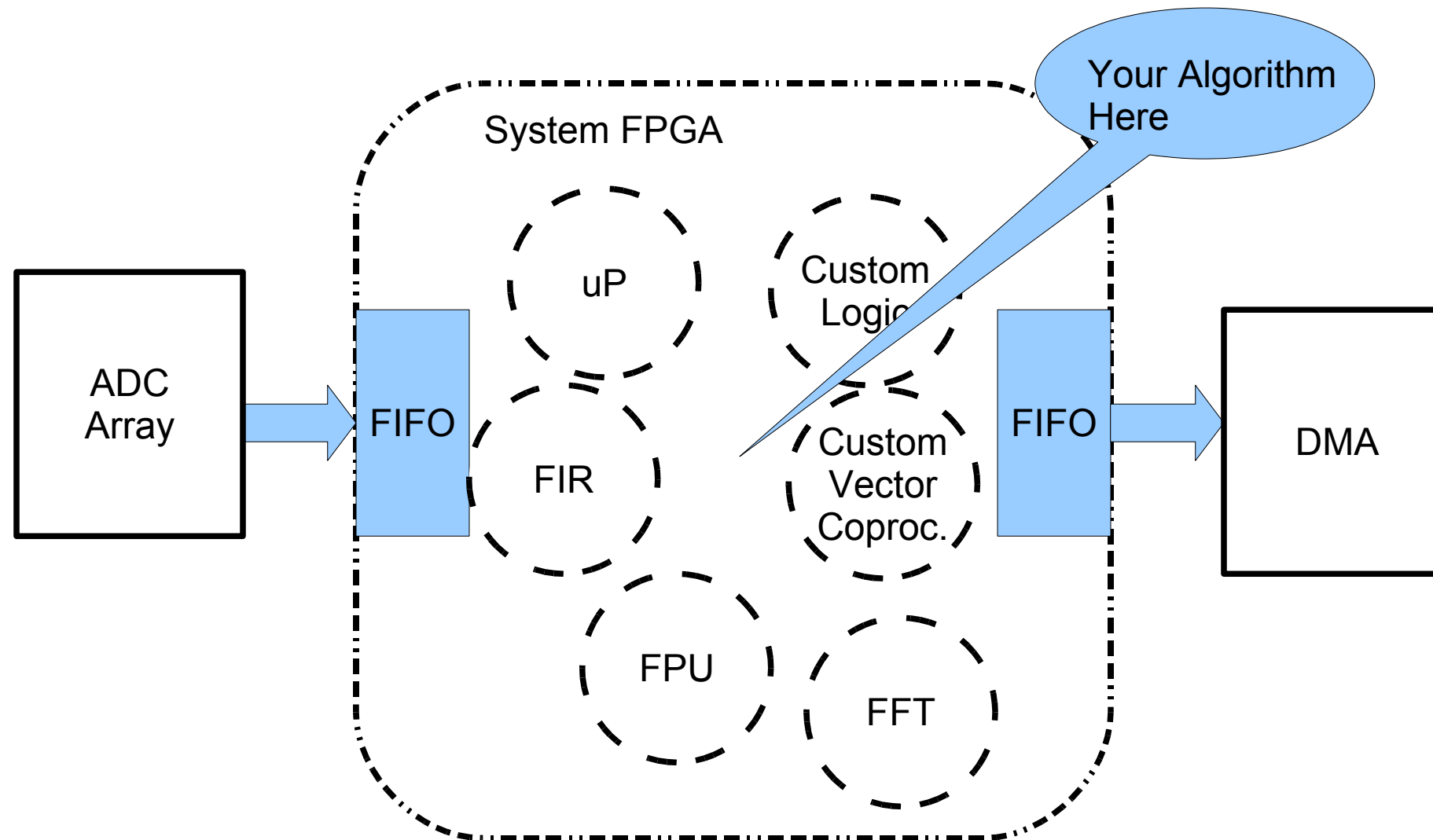
Each Klystron is managed by an ACQ216CPCI digitizer, monitoring 10 channels at 6MS/s and gating the Klystron by means of a Fiber Optic signal from a custom Rear Transition Module RTM.

The Trip and other handshake signals are shared between FPGA and CPLD (A), between devices using the PXI signaling backplane (B) and via off-crate connector (C). One device signaling a trip trips all devices simultaneously. Trip computed in less than 10usec.

All thresholds and ratios are pre-programmed before the shot, and all captured data, together with computation results, is uploaded to MDSplus after the shot. The cards are self contained devices connected by Gigabit Ethernet.

Alternative : use an embedded processor

Software manages Data flow, Hardware co-processors transform the data.



- Possibility to instantiate an embedded microprocessor core in the FPGA.
- The core has fast, low latency access to data.
- What can you do with a 100MIPS core?. Well, first the data is presented in cache, second there is the possibility to connect the data to a dedicated math accelerator unit – eg a hardware FFT function or a vector FPU.. and it's possible to have more than one embedded core.
- The vendor supplies the co-processors.
- Expected applications include threshold detection, alarms, and control.
- Implement your algorithm in C using GNU tools ...

Conclusion

Local processing simplifies ...

- Possibilities for local data reduction offer big savings in data upload time and storage size.
- Possibilities for local processing on the data allow fast real time feedback, for alarms, or real time control inputs.
- In some cases, the full rate data is also available in memory for analysis and debug.
- Intelligent digitizer with embedded microprocessor, TCP/IP and Linux operating system make configuration, control, data handling and exception handling easy.
- The solution is highly scaleable, since every additional digitizer brings its own processor. Acquisition scales at the network rather than the bus level.

Intelligent Simultaneous Data Acquisition

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