

Analog Threshold Detect (ATD) User Guide



High Performance Simultaneous Data Acquisition

Reference document for details relating to D-TACQ Analog Threshold Detect DSP Module

Revision History

Revision	Date	Author(s)	Description
1	28/10/2024	SR/PGM	Created

Contents

- 1 ATD Functional Summary 3**
- 2 Thresholds 4**
 - 2.1 Threshold Scale 4
 - 2.1.1 Minimum Resolution 4
 - 2.1.2 Bitshift for greater resolution 5
- 3 ATD EPICS Interface 6**
- 4 Interrupts and Events - HW/SW Interaction 15**

1 ATD Functional Summary

Programmable per channel threshold function, EPICS PVs are provided for all of:

- M: Mode Rising, Falling, Inside, Outside
- L1 : threshold for Rising, Falling
- L1 and L2 : limits for Inside, Outside.
- H : Hysteresis.

Standard DSP behaviour is to emit an EVENT on the first of any threshold crossings. This event may be used in several ways.

- To trigger a "live scope" display
- As the trigger in a PRE/POST capture to the limit of memory, eg in the Fault Monitor application
- In a streaming application, the Events are embedded in the data stream for remote processing

Grouping: the DSP logic triggers on first of many, always. However it's possible to group multiple triggers together, and allow embedded software to trigger the system. Grouping includes:

- Group CURRENT : all channels in group need to be active at the same time to output a trigger.
- Group HISTORY: trigger is emitted when all channels in group have been active since the previous trigger.
- Group FIRST_N: trigger when the first-n channels in the group are active (CURRENT mode) or have been active (HISTORY mode).

Events - the capture system must be configured to respond to the appropriate event:

- The DSP will typically emit EVENT.d0
- The ESW will emit EVENT.d1

In a DISTRIBUTED SCOPE application, the EVENT can be used to trigger a White Rabbit Trigger, to cause all units to trigger at time shortly in the future, then each unit stops, and rewinds time in the memory buffer to the exact moment of trigger. Any participating box in the distributed scope can declare a threshold crossing trigger, and trigger the entire fleet.

2 Thresholds

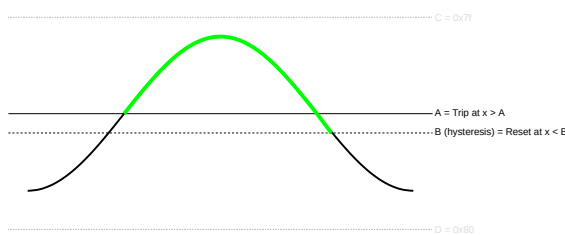
There are four 8-bit thresholds per channel. These are organised within a 32-bit quantity as follows :

0xAABBCCDD

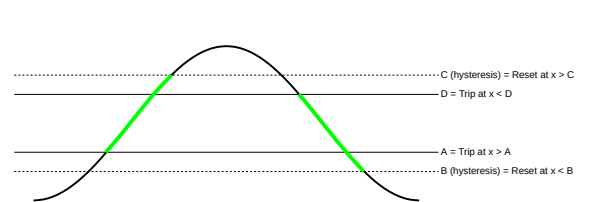
- AA = Bits 31 down to 24
- BB = Bits 23 down to 16
- CC = Bits 15 down to 8
- DD = Bits 7 down to 0

The selected function can be inferred by the logic based on the state of these thresholds. For a rising or falling test, two of the unused threshold values are set to ±full-scale.

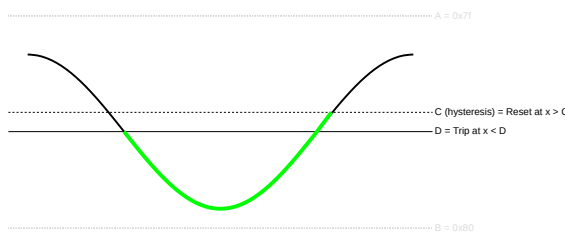
Rising : Thresholds 0xAABB180; A must be > than B



Inside : Thresholds 0xAABBCCDD; D must be > than A



Falling : Thresholds 0x7F80CCDD; C must be > than D



Outside : Thresholds 0xAABBCCDD; B must be > than C



Figure 1: Diagram showing the 4 supported threshold conditions

The hystereses in these examples are purposely exaggerated for clarity.

2.1 Threshold Scale

2.1.1 Minimum Resolution

ADC resolution for a ±10 V, 16-bit ADC :

$$\frac{20}{2^{16}} = 305 \mu\text{V}$$

8 MSBs of comparison gives us a minimum resolution of :

$$2^8 \times 305 \times 10^{-6} = 78 \text{ mV}$$

N.B. As an example, for the rising edge case, one would have to **clear the threshold by at least the minimum comparison resolution** to trip the ATD.

2.1.2 Bitshift for greater resolution

Shift Left	Scale	Maximum	Minimum Resolution
0	1	10 V	78 mV
1	2	5 V	39 mV
2	4	2.5 V	20 mV
3	8	1.25 V	10 mV

Table 1: Lorem ipsum

3 ATD EPICS Interface

ATD: Analog Threshold Detect
Live Scope with up to NCHAN triggers.

Default personality NCHAN=64
(2 x ACQ423ELF-32-200)

NCHAN can be 4..192

Supported on ACQ42x, ACQ43x, ACQ465

Definition: [4GUG](#): #13.3

EPICS PV's

1.0	\${UUT}:\${S}:ANATRG:\${CC}:M	enum	Mode. none rising falling inside outside	Prms For One Channel set immediate
1.1	\${UUT}:\${S}:ANATRG:\${CC}:H	enum	Hysterisis % 1 2 5 10 20	
1.2	\${UUT}:\${S}:ANATRG:\${CC}:L1	double	Level 1 V	
1.3	\${UUT}:\${S}:ANATRG:\${CC}:L2	double	Level 2 V	
2.0	\${UUT}:\${S}:ANATRG:ALL:M H/L1/L2	enum/ double	Parameters as above	Prms For ALL CH Commit with SET
2.1	\${UUT}:\${S}:ANATRG:ALL:SET	bo	SET all channels to ALL:M H/L1/L2	
3	\${UUT}:\${S}:ANATRG:LIVE:\${CC}	bi	Live State monitor	
4.0	\${UUT}:\${S}:ANATRG:GROUP:\${CC}	bo	Channel \${CC} is part of GROUP	
4.1	\${UUT}:\${S}:ANATRG:GROUP:ALL:SET	bo	Set all channels in Group	
4.2	\${UUT}:\${S}:ANATRG:GROUP:ALL:CLR	bo	Clear all channels from Group	
4.3	\${UUT}:\${S}:ANATRG:GROUP_MODE	enum	CURRENT (active same time) HISTORY (active in period)	
4.4	\${UUT}:\${S}:ANATRG:GROUP:FIRST_N	int	Trigger on first N channels in group.	
5	\${UUT}:\${S}:ANATRG:SCALE	enum	1,2,4,8 : 1:level is -127..+127 <<8, <<7, <<6, <<5 le as scale rises, level is closer to zero and more precise.	
6	\${UUT}:\${S}:ANATRG:RESET	bo	Reset all logic.	
\${UUT} : UUT NAME, \${S} : Site 1..6 \${CC} Channel 01..192				

Event Source Selection

ACQ400_LAUNCHER.opi capture.opi acq400sync.opi acq1102_00

acq1102_009 SYNC SYNC_ROLE master 200000

EXT SYNC BUS [HDMI]

CLK TRG SYNC GPIO

Main Timing Highway Source Routing

	d0	d1
CLK	EXT	MCLK
TRG	EXT	STRIG
SYNC	EXT	EXT

MISync Out Sel

	CLK	d1
CLK	CLK	d1
TRG	TRG	d2
SYNC	SYNC	d2
GPIO		d0

EXT SYNC BUS OUT [HDMI]

CABLE PRESENT

CLK TRG SYNC GPIO DRVEN

Event Bus Source

d0	d1	d2	d3	d4	d5	d6	d7
MOD	TRG	TRG	TRG	TRG	TRG	TRG	TRG

From Panel

`#{UUT}:0:SIG:EVENT_SRC:0
EVT.d0 SRC set MOD (ATD DSP)`

`#{UUT}:0:SIG:EVENT_SRC:1
EVT.d1 SRC set TRG`

`#{UUT}:0:SIG:SRC:TRG:1 STRIG
TRG.d1 SRC set STRIG
(soft-trigger). The ATD Interrupt Routine sets
soft-trigger to drive the system`

Controls

anatrgr.opi 100%

acq1102_009:2 Analog Trigger Configuration

CH	Mode	Hysteresis %	Level 1 V	Level 2 V	TRG	Group
01	rising	1	1	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>
02	rising	1	2	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>
03	rising	1	3	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>
04	rising	1	4	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>
05	none	1	0	0	<input type="checkbox"/>	<input type="checkbox"/>
06	none	1	0	0	<input type="checkbox"/>	<input type="checkbox"/>
07	none	1	0	0	<input type="checkbox"/>	<input type="checkbox"/>
08	none	1	0	0	<input type="checkbox"/>	<input type="checkbox"/>

ALL none 1 0 0

 Group SET

 Group CLR

Group Mode CURRENT First_N 0

 RESET Scale 1

CURRENT|HISTORY

 FIRST_N

Set M, H, L1, L2 for one channel (Immediate)
 \${UUT}:\${S}:ANATRGR:\${CC}:M/H/L1/L2

Select Channel in Group

Status

Set Parameters, then press ALL to set ALL CC

Include Group ALL

Exclude Group ALL

Standard (Direct DSP) Triggers

Live pre-post, lazy update ~1Hz.

343688 Updates so far.

RAPID Post-only update, 50Hz possible.

We set our FG for a BURST mode Sine output, 10Hz repetition rate.

4 triggers enabled and active (all channels same signal), so it will simply trigger on the first detection.

Trigger on EVT.d0: ATD trigger at 10Hz (we have FG with a 10Hz burst set up).

EVT.d1 : no events.

Trigger on EVT.d0 (DSP Direct)

acq1102_009:1 Analog Trigger Configuration

CH	Mode	Hysteresis %	Level 1 V	Level 2 V	TRG	Group
01	rising	1	1	0	Green	
02	rising	1	2	0	Green	
03	rising	1	3	0	Green	
04	rising	1	4	0	Green	
05	none	1	0	0	Green	
06	none	1	0	0	Green	
07	none	1	0	0	Green	
08	none	1	0	0	Green	
ALL	none	1	0	0	Green	

acq1102_009:2 Analog Trigger Configuration

CH	Mode	Hysteresis %	Level 1 V	Level 2 V	TRG	Group
01	rising	1	1	0	Green	
02	rising	1	2	0	Green	
03	rising	1	3	0	Green	
04	rising	1	4	0	Green	
05	none	1	0	0	Green	
06	none	1	0	0	Green	
07	none	1	0	0	Green	
08	none	1	0	0	Green	
ALL	none	1	0	0	Green	

Group Trigger

The screenshot displays the CS-Studio interface with several key components:

- Top Panel:** Shows acquisition control for 'acq1102_009:LIVE'. A green box highlights the 'Capture acq1102_009 Stream Control' area, which includes a 'STOP' button and a 'RUN' button. A callout bubble points to this area with the text: "Live pre-post, lazy update ~1Hz."
- Waveform Plot:** A plot showing a signal in Volts (y-axis, -9.99 to 9.99) versus Samples (x-axis, 0 to 3999). The signal is zero until approximately sample 2200, where it rises to a peak of about 9V, then falls to a trough of about -9V, and returns to zero. A callout bubble points to the plot with the text: "4 triggers enabled and active In the group. Trigger when ALL SET."
- Trigger Configuration:** Below the plot, there are tables for trigger settings. A callout bubble points to the 'EVENT0' row with the text: "\${UUT}:1:EVENT0:DX = d1 Trigger on EVT.d1 (SW Interrupt)".
- Analog Trigger Configuration:** Two panels show 'acq1102_009:1 Analog Trigger Configuration' and 'acq1102_009:2 Analog Trigger Configuration'. Both show 8 channels (CH01-08) with 'Mode' set to 'rising' and 'TRG' status indicators. A callout bubble points to the 'EVT.d1' row in the first configuration with the text: "EVT.d1 : 10Hz".

Group Trigger 2

CS-Studio

File Edit Search CS-Studio Window Help

ACQ400_LAUNCHER.opi capture.opi acq400sync.opi acq1102_009:LIVE acq1102clktree.opi acq1102_009:LIVE acq1102_009:LIVE

Transient Stream BLT Stats DataFlow Slowmon Multi-Event Sync Role HUDP A B D

Capture acq1102_009 Stream Control

STOP 3.64GiB 0:02:39 [24.4MiB/s]

34 RUN

sample_cou 51301627228 199775 Hz

cope Mod	RunTime	Samples	Rate MB/s	Live Wf Rate
pre-post	153	30670848	26	0.000 Hz

Leade Typ SHORT 343271 ..cq1102_009:2 CH01:08 caldef Mask PAUSE

Aggregator Site 1:2 1 1 Sample Size 128

TRG	ena...	d1	rising	SELECT SOFT TR	ULSE SOFT TR
EVENT0	ena...	d1	rising	find Event IDLE	0 0
EVENT1	disa...	d0	falling	stack 480	none
RGM	OFF	d0	falling	RTM_TRANSEN	0 0 IDLE

acq1102ctr.opi

acq1102_009 .atch On PP!

CLK d0	CLK d1	CLK d2	CLK d3
0.000 Hz	1.998E5 H	1.998E5 H	0.000 Hz
0	5E10	5E10	0
EXT C	MB C	S1 C	S2 C
TTC d0	TTC d1	TTC d2	TTC d3
10.000 Hz	0.000 Hz	0.000 Hz	0.000 Hz
2E6	2E6	2E6	0
EXT C	MB C	S1 C	S2 C
EVT d0	EVT d1	EVT d2	EVT d3
10.000 Hz	0.000 Hz	0.000 Hz	0.000 Hz
2E6	2E6	2E6	0
EXT C	MB C	S1 C	S2 C
SYN d0	SYN d1	SYN d2	SYN d3
0.000 Hz	0.000 Hz	0.000 Hz	0.000 Hz
0	0	34	0
EXT C	MB C	S1 C	S2 C

acq1102_009:1 Analog Trigger Configuration

CH	Mode	Hysteresis %	Level 1 V	Level 2 V	TRG	Group
01	none	1	0	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>
02	none	1	0	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>
03	none	1	0	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>
04	none	1	0	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>
05	none	1	0	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>
06	none	1	0	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>
07	none	1	0	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>
08	none	1	0	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>
ALL	none	1	0	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>

Group Mode CURRENT First_N 0 RESET Scale 1

acq1102_009:2 Analog Trigger Configuration

CH	Mode	Hysteresis %	Level 1 V	Level 2 V	TRG	Group
01	rising	1	0	0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
02	rising	1	0	0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
03	rising	1	0	0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
04	rising	1	0	0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
05	none	1	0	0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
06	none	1	0	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>
07	none	1	0	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>
08	none	1	0	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>
ALL	none	1	0	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>

Group Mode CURRENT First_N 0 RESET Scale 1

4 triggers enabled and active.
5 triggers in the group.
Trigger when ALL SET.

EVT.d1 : 0Hz : One Group Trigger isn't happening

Group Trigger 3

The screenshot displays the CS-Studio interface with several key components:

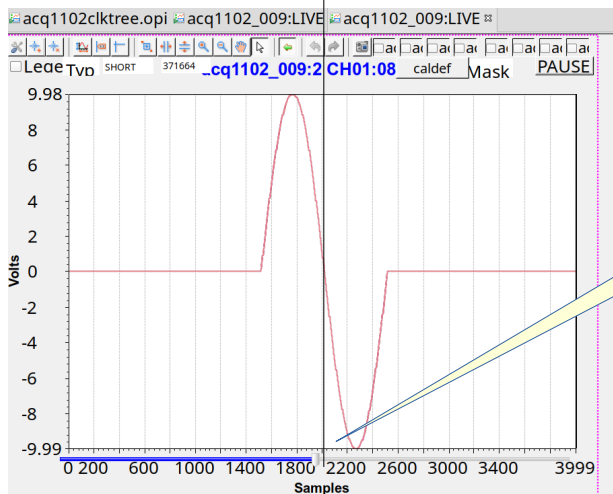
- Top Left Panel:** 'Capture acq1102_009 Stream Control'. It shows a 'STOP' button, a progress bar at 34%, and a 'Live Wf Rate' of 1,000 Hz. A yellow callout bubble points to this area with the text: "Live pre-post, lazy update ~1Hz."
- Top Right Panel:** A waveform plot showing 'Volts' on the y-axis (ranging from -9.99 to 9.99) and 'Samples' on the x-axis (ranging from 0 to 3999). The plot shows a single pulse centered around sample 2200.
- Bottom Left Panel:** 'acq1102ctr.opi' showing a table of trigger configurations for 'acq1102_009'. A yellow callout bubble points to the 'EVT.d1' field with the text: "EVT.d1 : 10Hz : restored".
- Bottom Middle Panel:** 'acq1102_009:1 Analog Trigger Configuration'. It contains a table for channels CH01-08.
- Bottom Right Panel:** 'acq1102_009:2 Analog Trigger Configuration'. It contains a table for channels CH01-08.

EVT.d1 : 10Hz : restored

Set FIRST_N to 4: we have 4 live triggers in the set, so the system triggers.



Live Delay Control



PRE=POST

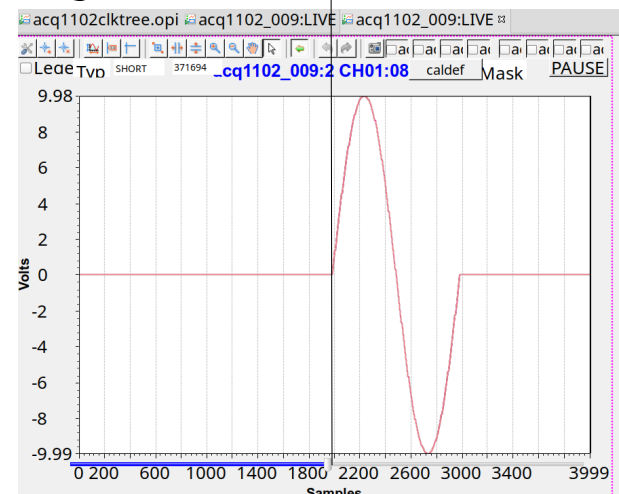
falling

falling

anatrgr.opi

acq1102_009:2 Analog Trigger Configuration

CH	Mode	Hysteresis %	Level 1 V	Level 2 V	TRG	Group
01	falling	1	1	0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

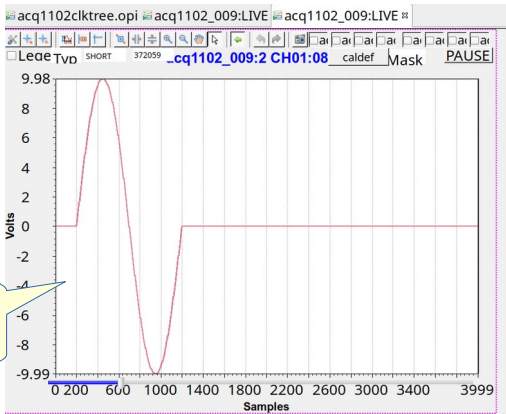


anatrgr.opi

acq1102_009:2 Analog Trigger Configuration

CH	Mode	Hysteresis %	Level 1 V	Level 2 V	TRG	Group
01	rising	1	1	0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

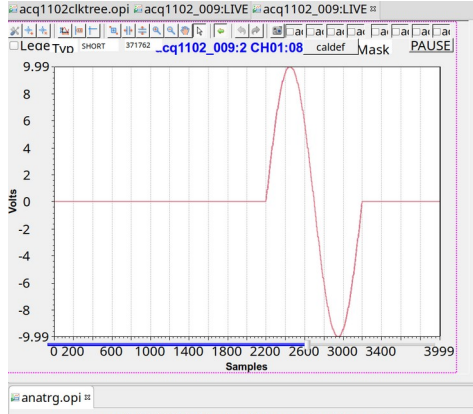
Live Delay adjust: 0..100%
 $\{\text{UUT}\}:\text{LIVE}:\text{PREPCT}$



anatrgr.opi

acq1102_009:2 Analog Trigger Configuration

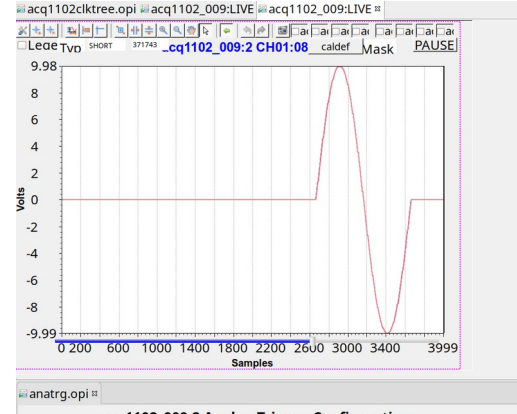
CH	Mode	Hysteresis %	Level 1 V	Level 2 V	TRG	Group
01	falling	1	1	0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>



anatrgr.opi

acq1102_009:2 Analog Trigger Configuration

CH	Mode	Hysteresis %	Level 1 V	Level 2 V	TRG	Group
01	falling	1	1	0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>



anatrgr.opi

acq1102_009:2 Analog Trigger Configuration

CH	Mode	Hysteresis %	Level 1 V	Level 2 V	TRG	Group
01	rising	1	1	0	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

4 Interrupts and Events - HW/SW Interaction

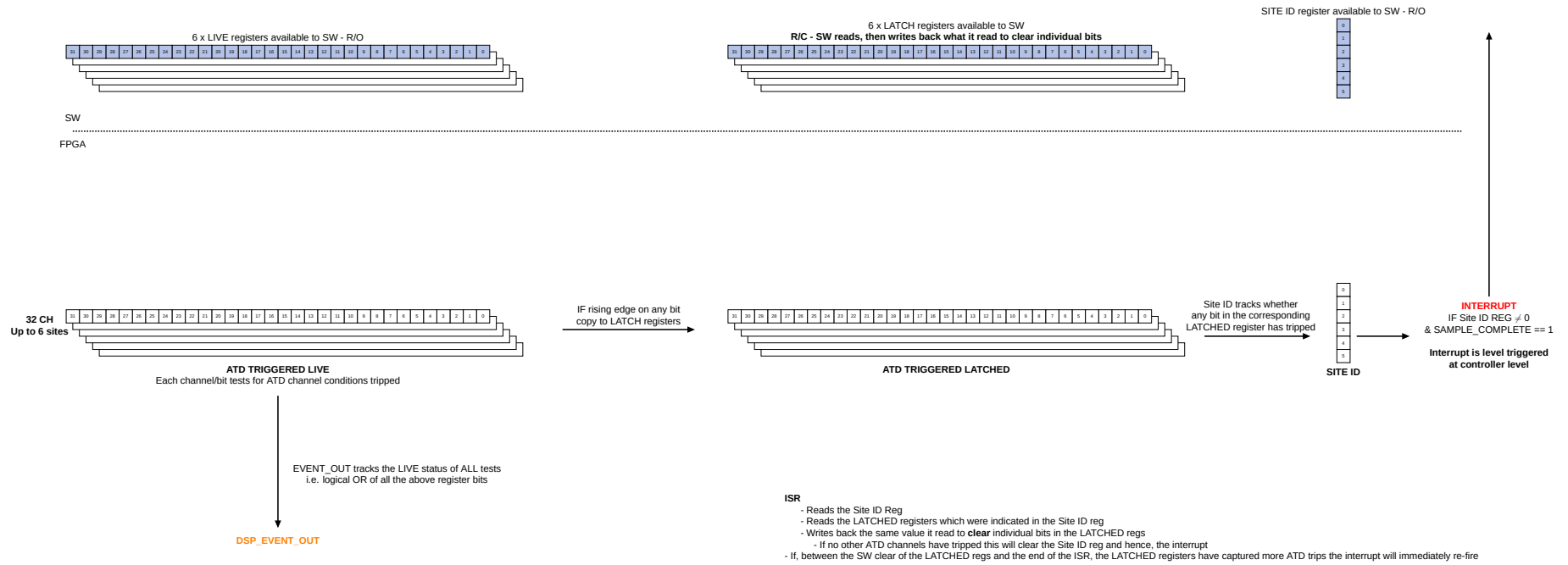


Figure 2: Illustrating the Event and Interrupt interaction between HW and SW