ATD : Analog Threshold Detect Test/FAT

- ATD is an FPGA DSP feature that provides an Analog Trigger

- We demo a scope, with a "normal" external digital trigger, and an analog trigger, like a "normal" scope.

- However this scope has 64 channels, and any or all channels can declare an analog trigger event.

- Each trigger channel has programmable LEVEL, EDGE, hysterisis.

- Trigger options include RISING, FALLING, INSIDE, OUTSIDE.

- Triggers may be "RAW": first channel to trigger, or grouped, group triggers may be "CURRENT" (at same time) or "HISTORY" (cumulative). Group trigger on "ALL" or "FIRST_N" triggers.

- DSP logic scales 4..192 channels, 200..2000kSPS/channel.
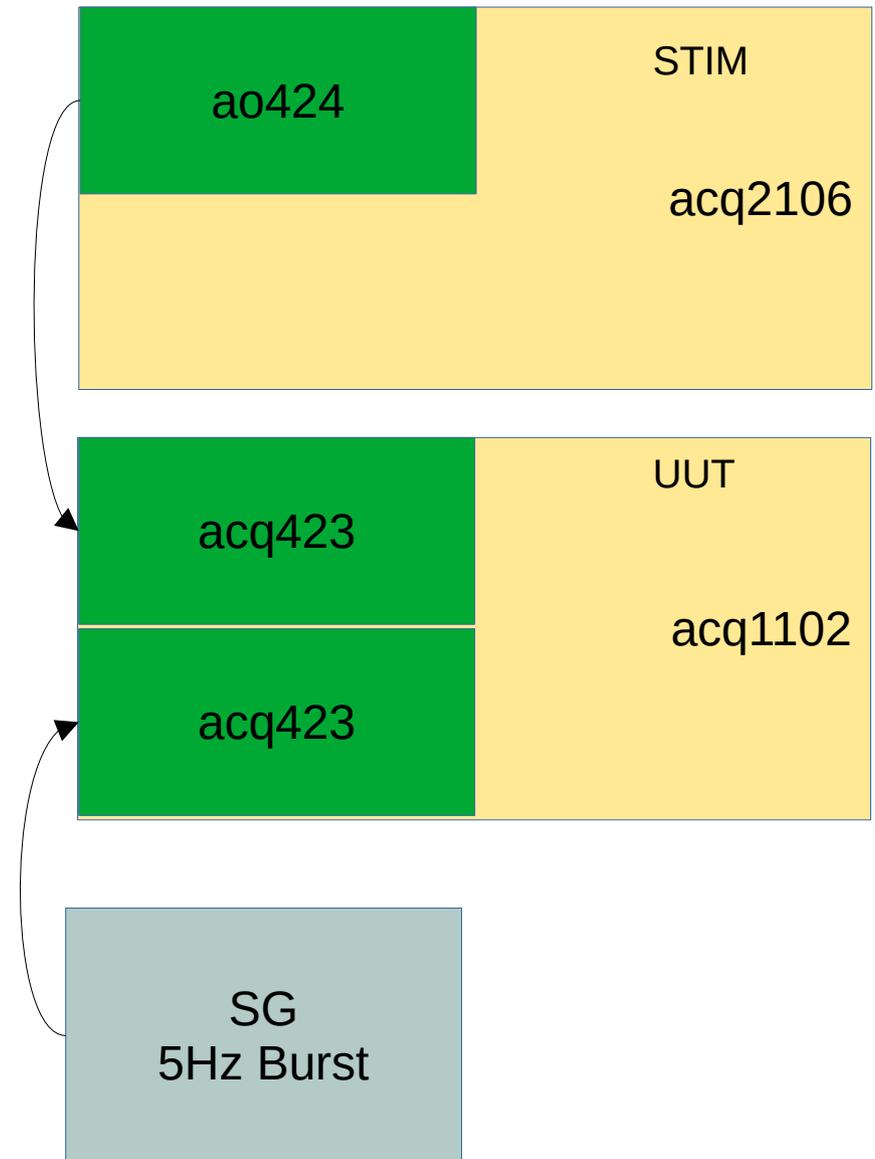
D-TACQ Solutions

ATD : Analog Trigger: Test Setup

We demonstrate ATD on a
System with 64AI.

We chose ACQ1102 with 2xACQ423,
however ATD will scale to any ACQ42x ADC
system, 4..192 channels.

System setup

Connect ao424 to acq423[1]
Connect SG to acq423[2]
Connect SG sync to the TRG input on both units

STIM

ao424

acq2106

UUT

acq423

acq1102

acq423

SG
5Hz Burst

D-tAcq
Solutions

ATD Supported release

⚠ Not secure acq1102_009/d-tacq/#id

| Home | System | Firmware | FPGA | Temperature | Power | Status | Top | Interrupts | hudp |

```
CARRIER
SITE        MANUFACTURER        MODEL                           PART            SERIAL
  0         D-TACQ Solutions    acq1102                         acq1102         CE4120009

build detail: root@rpi-009 R1010 Tue Apr 09 14:47:20 UTC 2024
eth0 macaddr: 00:21:54:10:00:09   eth0  ipaddr: 10.12.197.147

MODULES
SITE        MANUFACTURER        MODEL                           PART            SERIAL
  1         D-TACQ Solutions    ACQ423ELF   ACQ423ELF-32-200-16-FFC N=32 M=09   E42310001
  2         D-TACQ Solutions    ACQ423ELF   ACQ423ELF-32-200-16-FFC N=32 M=09   E42310002
```

acq1102_009   Sat Nov 30 20:48:24 UTC 2024

⚠ Not secure acq1102_009/d-tacq/#fw

| Home | System | Firmware | FPGA | Temperature | Power | Status | Top | Interrupts | hudp |

```
RELEASE acq400-725-20241130191533
RELEASE : /tmp/release.md5
CURRENT : /tmp/current.md5
Base file system /etc/acq400_version:
acq400_buildroot acq400_v2024.02 pgm@hoy6 Wed  7 Aug 08:58:09 BST 2024 6d9e3a595c7216d36683808aa545
RELEASE acq400-725-20241130191533
Clean Release Installed
/mnt/ko/fpga-725-20241130191533.img
ESW and GW DATECODES 20241130191533 MATCH: GOOD
```

acq1102_009   Sat Nov 30 20:49:24 UTC 2024

⚠ Not secure acq1102_009/d-tacq/#fpga

| Home | System | Firmware | FPGA | Temperature | Power | Status | Top | Interrupts | hudp |

```
load.fpga loaded /mnt/ACQ1102_TOP_09_09_9802_U_W_32B.bit.gz
xiloader r1.01 (c) D-TACQ Solutions
eoh_location set 0
Xilinx Bitstream header.
built with tool version   : 40
generated from filename   : ACQ1102_TOP_09_09_9802_U_W_32B
part                      : 7z030fbg676
date                      : 2024/10/17
time                      : 15:46:12
bitstream data starts at  : 126
bitstream data size       : 5979916
```

acq1102_009   Sat Nov 30 20:50:01 UTC 2024

Install software on host

1) Install HAPI

```
> mkdir PROJECTS
> cd PROJECTS
> git clone https://github.com/D-TACQ/acq400_hapi
> cd acq400_hapi
> pip3 install -e .
```
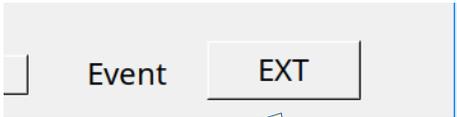
Recommended UI Layout

Trigger Signal Routing

One controls sets it all:
${UUT}:1:ANATRG:SRC_SEL

Event EXT

Regular FP Digital Trigger

EVENT0	ena...	d0	rising	Find E
EVENT1	disa...	d0	falling	

GPIO

Event Bus Source

d0	d1	d2	d3	d4
TRG	TRG	TRG	TRG	TRG

Event ATD_RAW

DSP MODule (ATD) Trigger
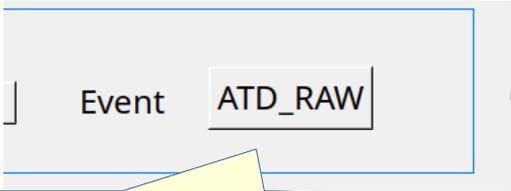
EVENT0	ena...	d0	rising
EVENT1	disa...	d0	falling

Event Bus Sou

d0	d1
MOD	TRG	T

Event ATD_GRP

Group Trigger, synthetic signal on TRG.d1
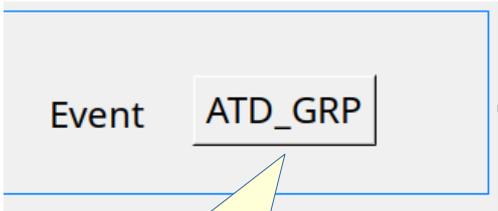
TRG	ena...	d1	rising
EVENT0	ena...	d1	rising
EVENT1	disa...	d0	falling

Event Bus

d0	d1
MOD	TRG

D-tAcq Solutions

STIM Demo Program

- ./test_apps/anatrg_demo.py --ai=acq1102_009 --ao=acq2106_133

- Plays a sequence of walking impulse responses.
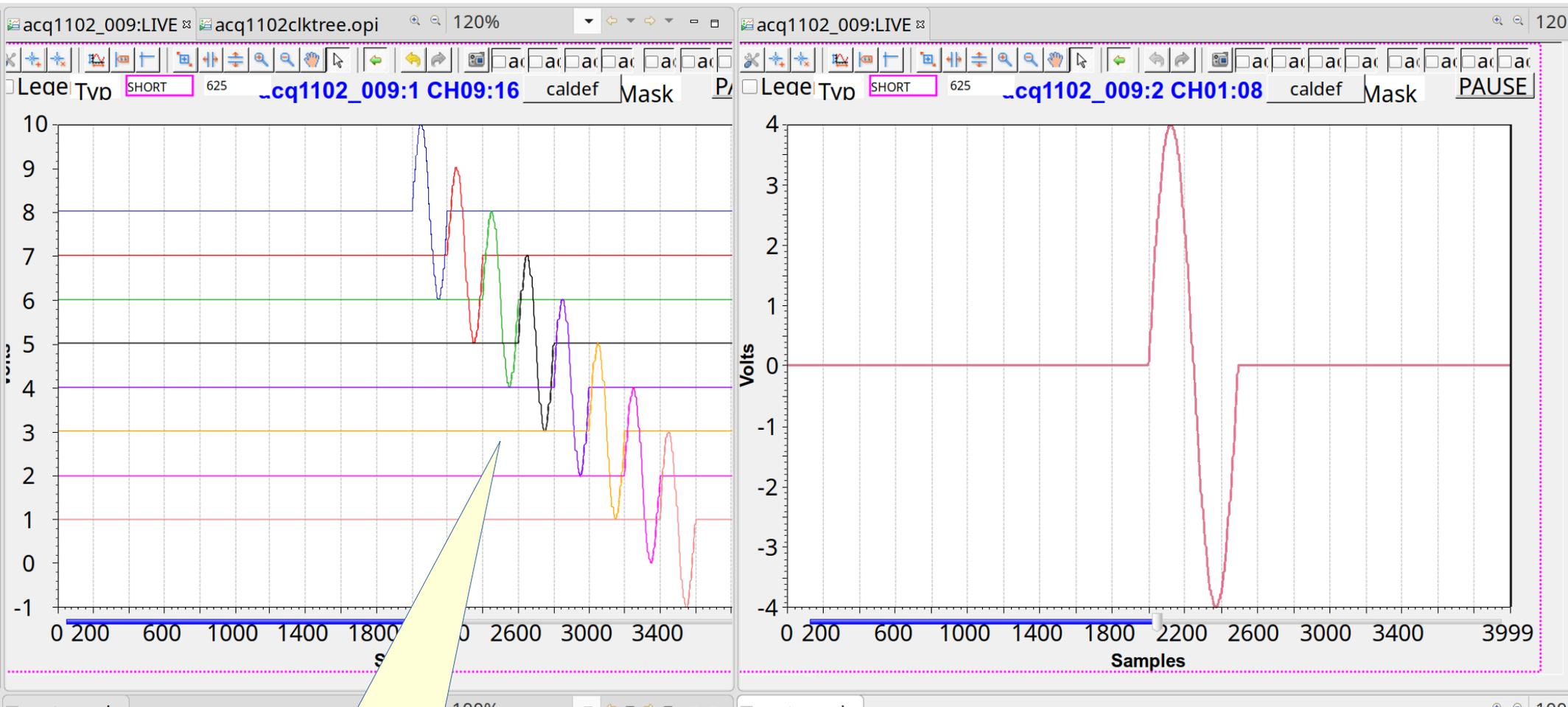
8 Channel pattern, repeated 8x over one channel at a time. Patter is duplicated over 32ch

Stim Demo Digital Trigger
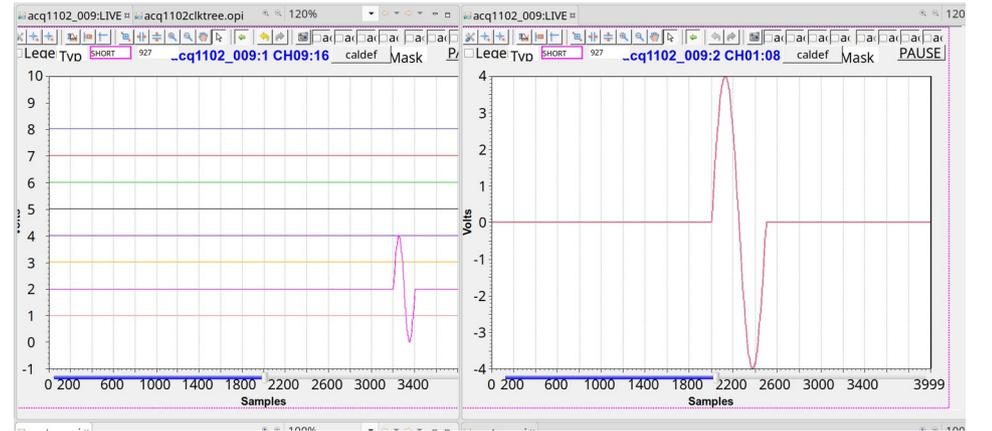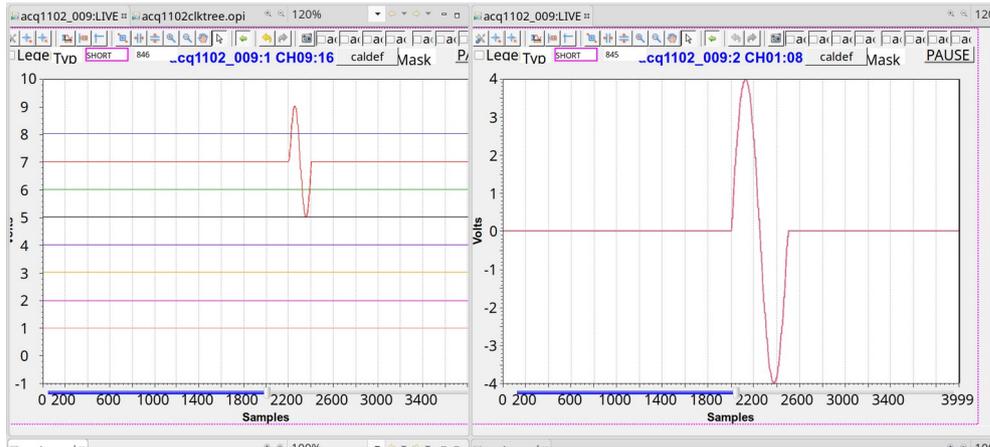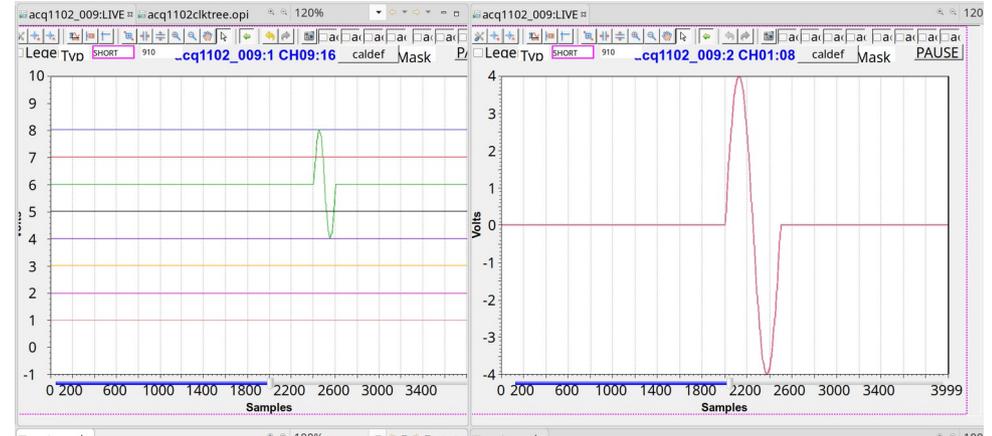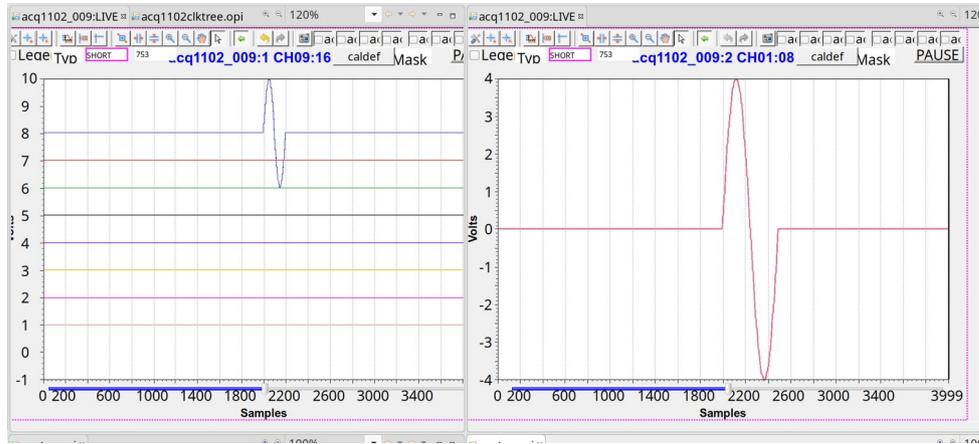
Digital Trigger, constant phase
The pulse on the left screen walks across
in time (as per pattern).
The cycle on the right screen IS
Constant phase wrt TRG and stays in a
constant position

Event   EXT

Copyright © D-TACQ Solutions Ltd 2024

ATD Group

Analog Group trigger only fires
For the combo waveform, it's the only
time all waveforms are active in the
HISTORY buffer..

Stim Demo: Analog Trigger
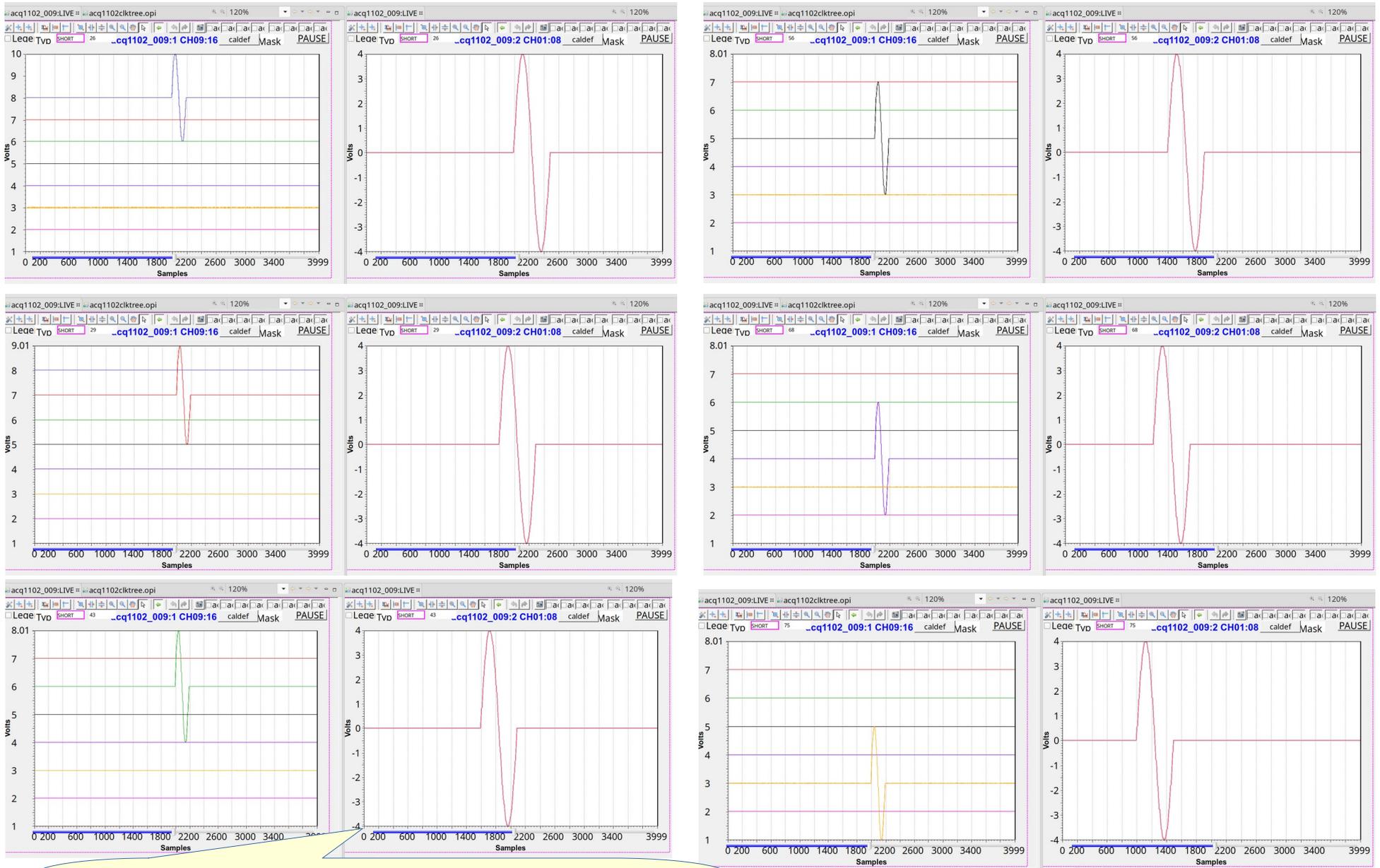
Analog Trigger: constant threshold
Variable phase AWG WF stays at Constant mid-screen,
fixed phase SG WF walks left.

Testing triggering rates

Generate 4 repeating waveforms with different wavelengths

```
./user_apps/utils/wavegen.py --wavelength=6000,12000,24000,48000 \
   --cycles=8 --nchan=32 --save=4freqs
```

```
awg_continuous 32CH.2B.48000.8CYCL.4freqs.dat
```


32CH.2B.48000.8CYCL
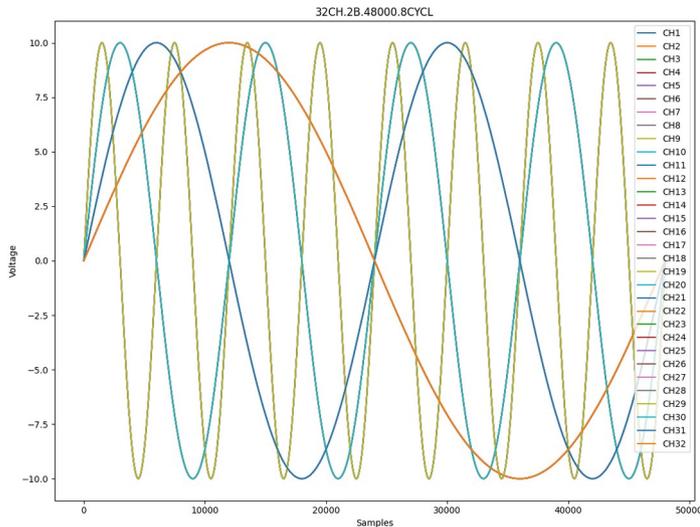
CH	Mode	Hysterisis %	Level 1 V	Level 2 V	TRG	Group
01	rising	1	8	0		✓
02	rising	1	8	0		
03	rising	1	8	0		
04	rising	1	8	0		

Trigger rate is half the previous

Enable a group at a time

NB: Trigger rate maxes out at 100Hz

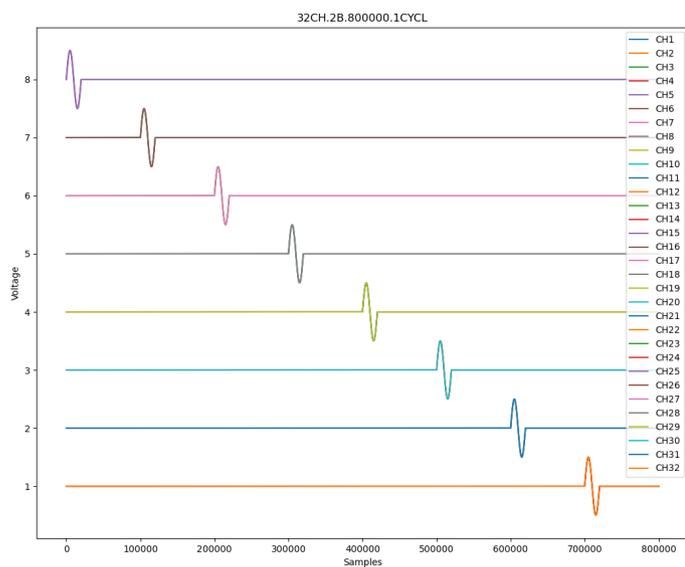| TRG.d1	TRG.d1	TRG.d1	TRG.d1
83.000 Hz Clo:	42.000 Hz	20.000 Hz	11.000 Hz
4E4	4E4	4E4	4E4
MB C	MB C	MB C	MB C

Testing trigger levels and history mode

Generate 1V sines offset by 1V and 100k samples apart

```
./user_apps/utils/wavegen.py --nchan=32 --scale=0.05 --offset=+8:1,-1 --totallength=800000 \
    --spos=+1:800000,100000 --save=offsetXY
```

```
awg_continuous 32CH.2B.800000.1CYCL.offsetXY.dat
```


Each channel triggers in sequence

Enable history mode and check D1 triggers only after all channels get triggered in sequence
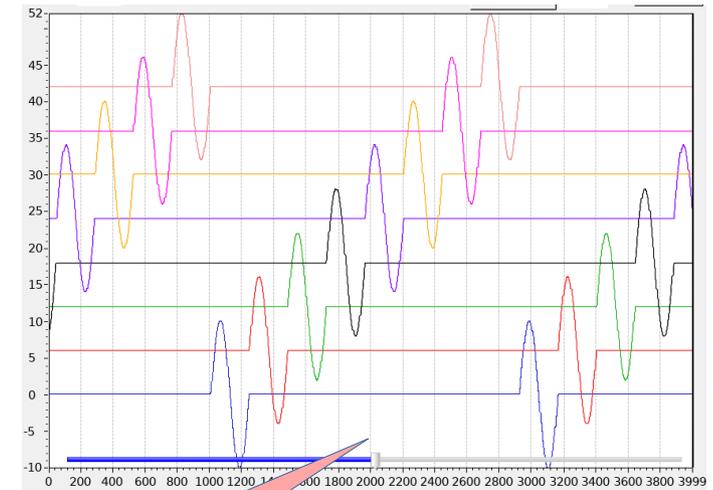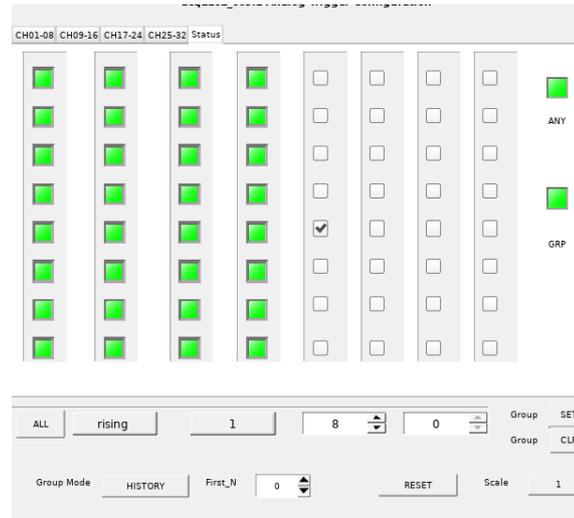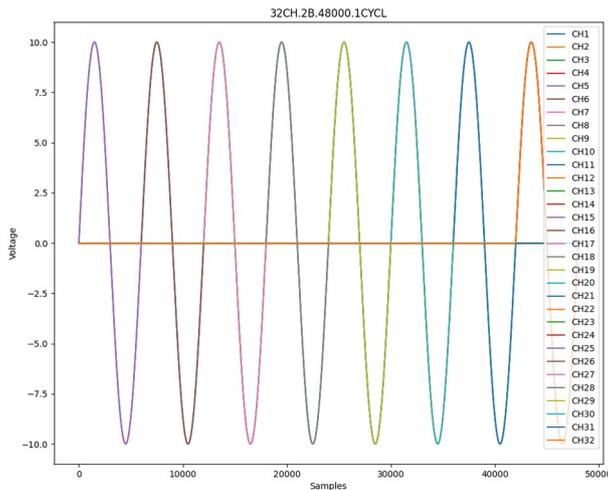
Testing trigger event position

Generate sines spaced after the previous

```
./user_apps/utils/wavegen.py --nchan=32 --scale=1 --totallength=48000 --wavelength=6000  \
    --spos=+1:48000,6000 --save=offsetX
```

Enable waterfall

```
/usr/local/epics/scripts/set.AI.waterfall
```

```
awg_continuous 32CH.2B.48000.1CYCL.offsetX.dat
```
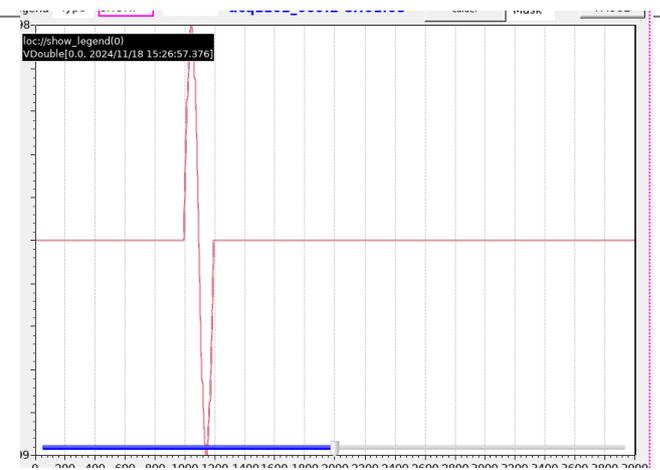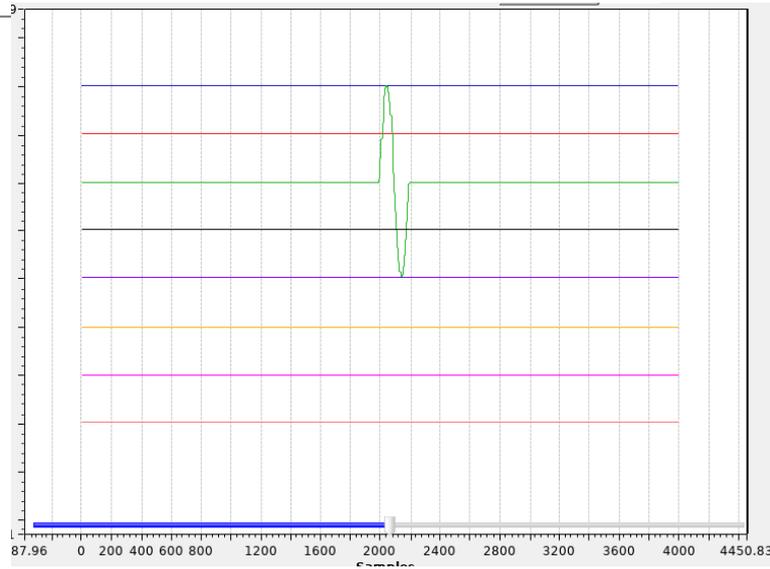

Event at channel 5 sine

Running trigger source demo

Run demo from hapi

```
./test_apps/anatrg_demo.py --ai=acq1102_009 --ao=acq2106_133
```

When event bus source is MOD plot is centerd on awg output

When event bus source is TRG plot is centered on SG output